TA660 Device Compliance Test

User's Guide

Scope

The scope of this document is to familiarize the user with various sections of the Device Compliance Test where IUT interaction is required. This document should allow the user to prepare for these tests in advance.

Description

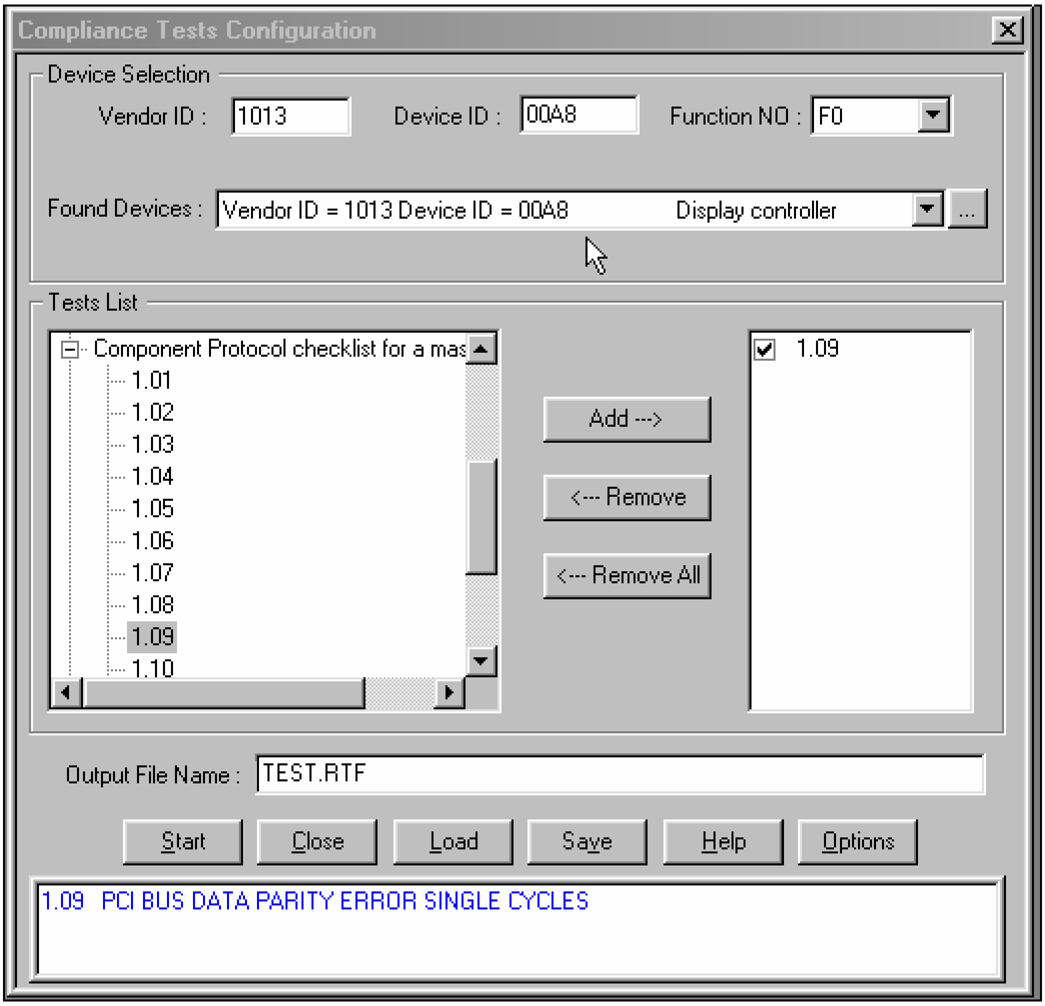
Compliance Test program includes three test categories which require interaction from IUT. These are DS_XX (device status test), MP_XX (General Component Protocol checklist of master) and 1.XX (Component Protocol checklist for a master device) tests. All other tests are performed automatically.

In these tests the TA660 is used as target and the IUT is the master. The TA660 as a target device needs to have three different addresses for Memory, I/O and Configuration spaces where master (IUT) can read and write to these addresses. These addresses must be free from use by other agents in the system therefore the TA660 software searches the system at the beginning of the compliance test and finds the addresses which TA660 can use. So long as the system under test has not changed configuration these addresses should stay the same for use for TA660 during the Device Compliance Test.

Most of the time the Memory address found for TA660 is at 0x10000000 and free I/O address is at 0x10000000. Please note this may change depending on system configuration and address assignment by the BIOS.

To find which addresses are free for TA660 as target in advance the user may select and execute test 1.09 (press cancel at each message not to execute the test if only verifying the address assignment for TA660).

In the example below all memory, I/O and Configuration addresses are all assigned to be 0x10000000



Compliance Tests Configuration

Device Selection

Vendor ID : 1013 Device ID : 00A8 Function NO : F0

Found Devices : Vendor ID = 1013 Device ID = 00A8 Display controller

Tests List

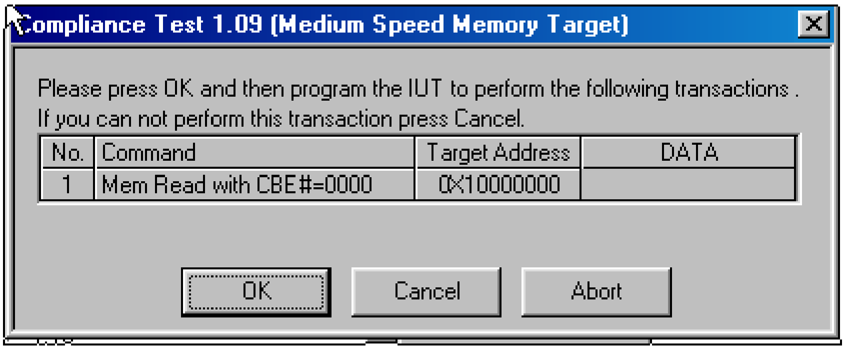
Component Protocol checklist for a mas
- 1.01
- 1.02
- 1.03
- 1.04
- 1.05
- 1.06
- 1.07
- 1.08
- 1.09
- 1.10

☑ 1.09

Output File Name : TEST.RTF

1.09 PCI BUS DATA PARITY ERROR SINGLE CYCLES

Test Selection menu

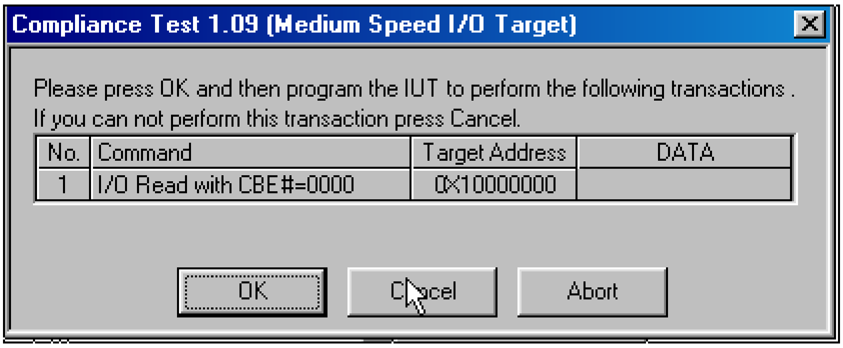


Compliance Test 1.09 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Read with CBE#=0000	0X10000000	

Memory address specified to be at 0x1000000

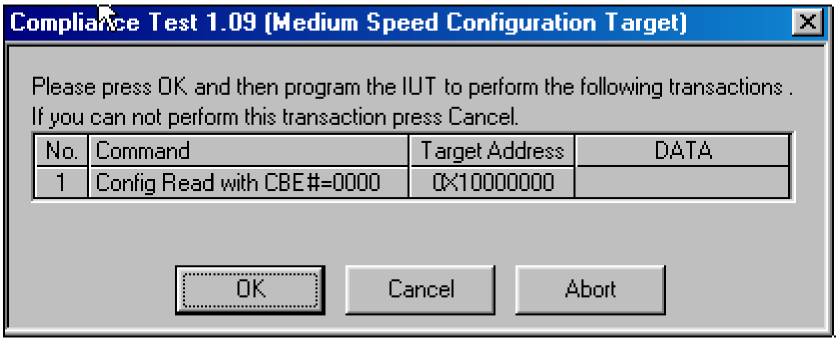


Compliance Test 1.09 (Medium Speed I/O Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	I/O Read with CBE#=0000	0X10000000	

I/O address specified to be at 0x10000000



Compliance Test 1.09 (Medium Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

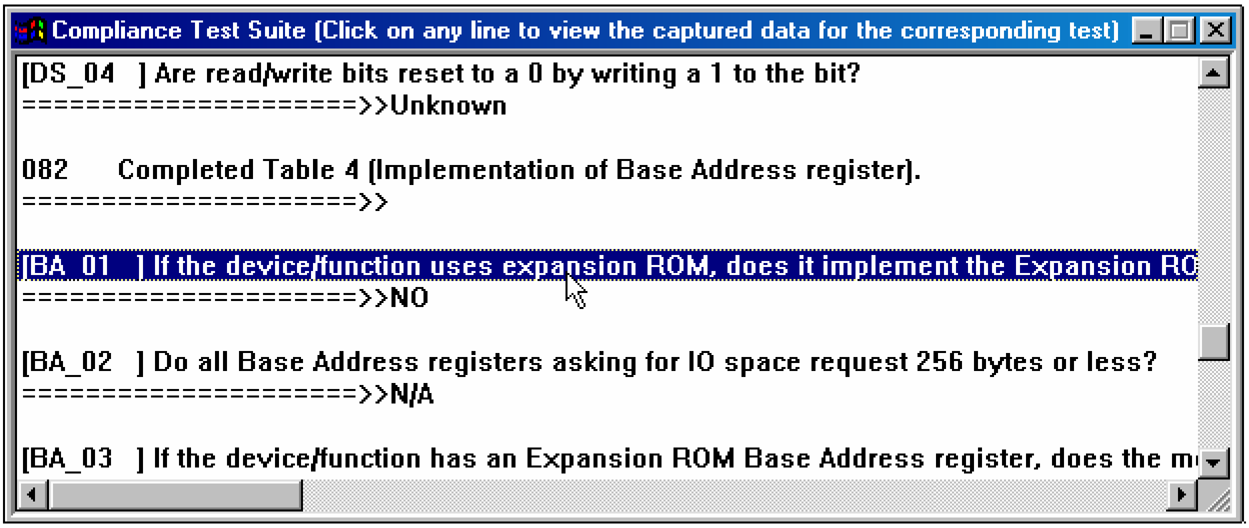
No.	Command	Target Address	DATA
1	Config Read with CBE#=0000	0X10000000	

Configuration address specified to be at 0x10000000

Pass/Fail

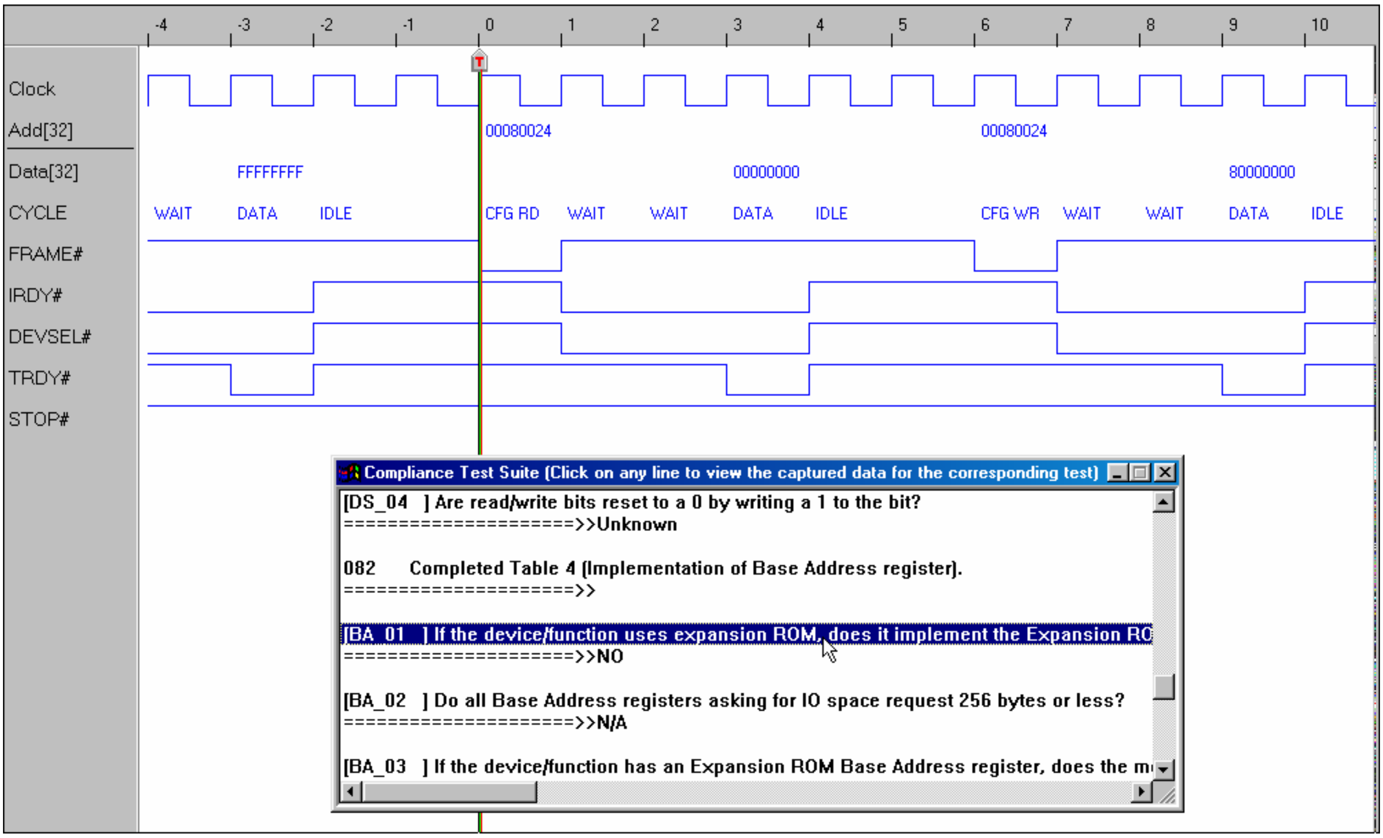
Pass/Fail of a test does not necessarily depend on Yes/No responses, some devices may be designed not to perform certain functions. Therefore the user must study the test response and compare it with its device specifications to see if it is okay or not.

In order to understand why TA660 reported a Yes or No response users may double click on the desired test title (on the screen display not the saved test report), BA-01 in this case, and a data display will open up corresponding to this test indicating the captured TA660 interaction with the IUT device. Most cases if the response has been No the trigger position will be on the transaction that has caused the No response.



Compliance Test Suite (Click on any line to view the captured data for the corresponding test)

```
[DS_04  ] Are read/write bits reset to a 0 by writing a 1 to the bit?
=====================>>Unknown

082     Completed Table 4 (Implementation of Base Address register).
=====================>>

[BA_01  ] If the device/function uses expansion ROM, does it implement the Expansion RO
=====================>>NO

[BA_02  ] Do all Base Address registers asking for IO space request 256 bytes or less?
=====================>>N/A

[BA_03  ] If the device/function has an Expansion ROM Base Address register, does the m
```



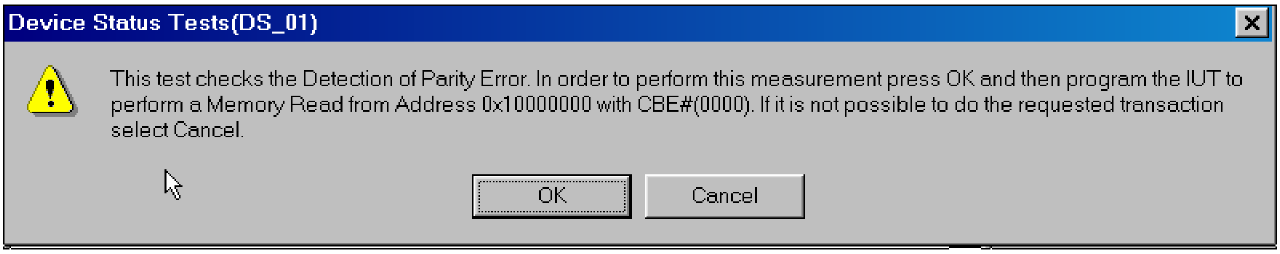
Compliance Test Suite (Click on any line to view the captured data for the corresponding test)

```
[DS_04   ] Are read/write bits reset to a 0 by writing a 1 to the bit?
====================>>Unknown

082      Completed Table 4 (Implementation of Base Address register).
====================>>

[BA_01   ] If the device/function uses expansion ROM, does it implement the Expansion RO
====================>>NO

[BA_02   ] Do all Base Address registers asking for IO space request 256 bytes or less?
====================>>N/A

[BA_03   ] If the device/function has an Expansion ROM Base Address register, does the m
```

Tests

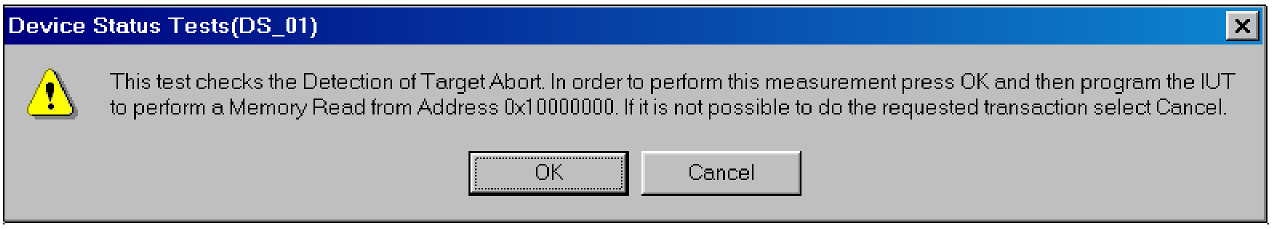
DS_XX

In this group there are three transactions to be executed requiring IUT interactions. These transactions are initiated by the messages indicated below:



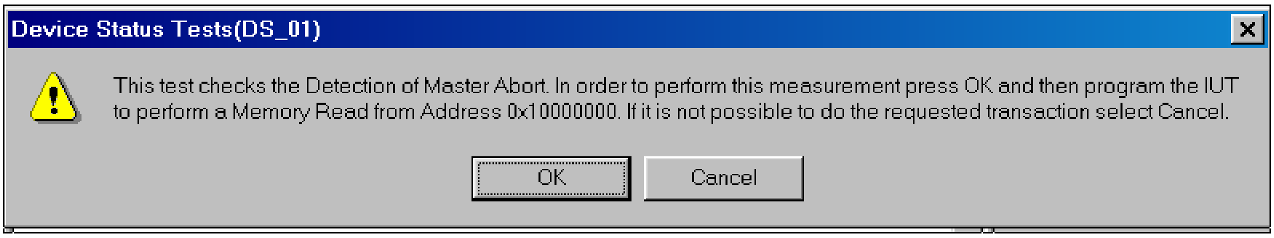
This test checks the Detection of Parity Error. In order to perform this measurement press OK and then program the IUT to perform a Memory Read from Address 0x10000000 with CBE#(0000). If it is not possible to do the requested transaction select Cancel.

Parity Error test



This test checks the Detection of Target Abort. In order to perform this measurement press OK and then program the IUT to perform a Memory Read from Address 0x10000000. If it is not possible to do the requested transaction select Cancel.

Master Detection of Target Abort



This test checks the Detection of Master Abort. In order to perform this measurement press OK and then program the IUT to perform a Memory Read from Address 0x10000000. If it is not possible to do the requested transaction select Cancel.

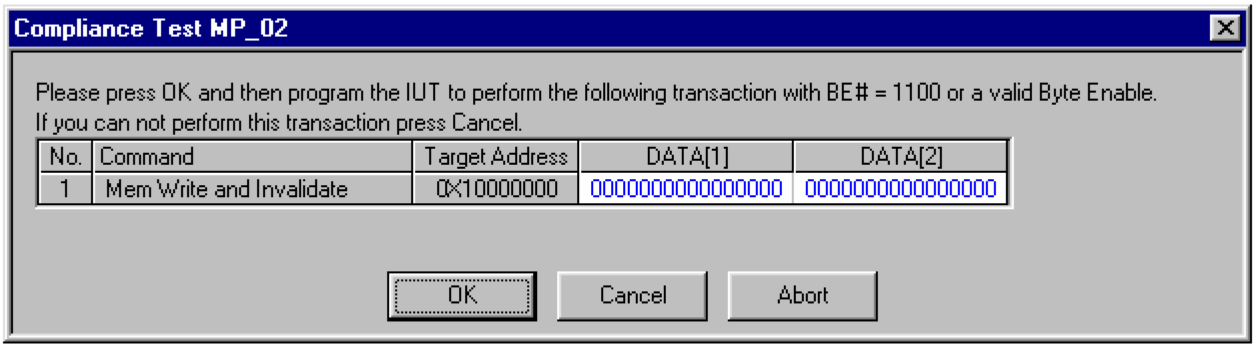
Master Abort due to Target not responding

As you see, the required transaction is a memory read from address 0x10000000H. This address is found by TA660 as a free address in memory space.

MP_XX
General Component Protocol checklist(master)

Most requests are for only one transaction as indicated here, these transactions may be a single word or a burst transfer. In this example a memory write and invalidate command with two data phases is requested.

The user may change the data in the white fields. For 32 bit bus set the upper bits to 00000000.

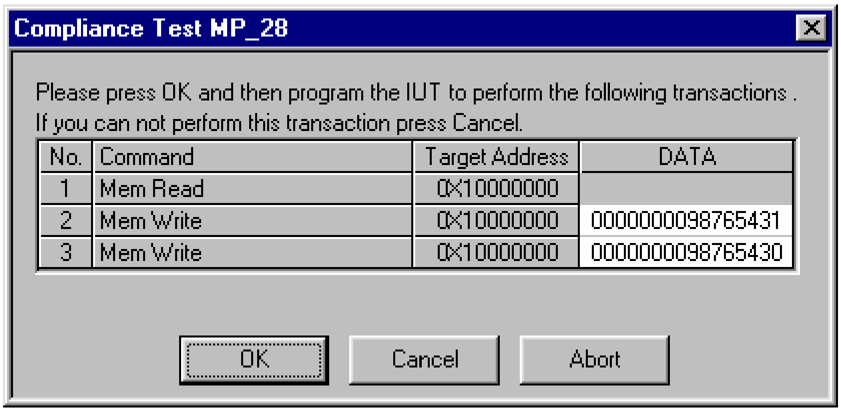


Compliance Test MP_02

Please press OK and then program the IUT to perform the following transaction with BE# = 1100 or a valid Byte Enable.
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write and Invalidate	0X10000000	0000000000000000	0000000000000000

Some requests require several transactions. In this example first a memory read and then two memory writes with different data are requested.

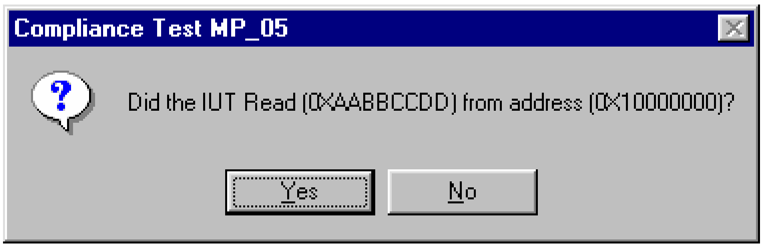


Compliance Test MP_28

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Read	0X10000000	
2	Mem Write	0X10000000	0000000098765431
3	Mem Write	0X10000000	0000000098765430

Sometimes the user is requested to confirm the result at the end of the test.



Compliance Test MP_05

Did the IUT Read (0XAABBCCDD) from address (0X10000000)?

MP Tests

General Component Protocol checklist (master)

Below are the list of requested transactions and their corresponding tests.

Please note that the addresses shown in the examples are based on the test setup, your system may result different addresses. Be sure to do test 1.09 to see what the addresses are free for each Memory, I/O and Configuration spaces.

Some of MP tests are interrelated, These tests are:

1. MP_06 - MP_07 - MP_14 - MP_15 - MP_16
2. MP_24 - MP_25
3. MP_28 - MP_29

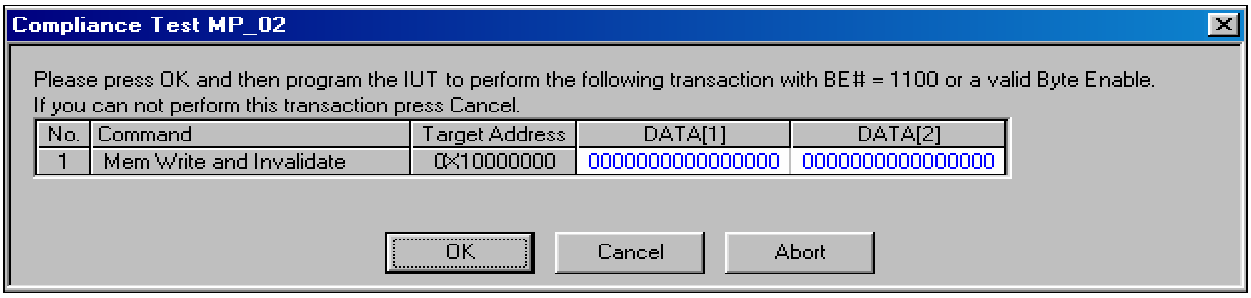
The required transactions for each set of tests are the same, thus once one of these tests is executed and the required transaction is performed there will be no message for the next test(s) to perform a transaction. For example to execute test MP_14 only, a message will ask for executing a memory read command with three data phases. But if tests MP_06 or MP_07 have been executed prior to MP_14 the software will not require the memory read transaction again when MP_14 is to be executed.

There is no priority for which test to be executed first. For example MP_25 may be executed first and then MP_24,and the software will only requests the transaction to be performed for the first test.

It should be noted that the title of the message box is always includes the name of the first test in the group, so even only MP_25 is executed the title will be “Compliance Test MP_24”.

- **MP_02**
  IUT always asserts all byte enables during each data phase of a Memory Write Invalidate cycle. (3.1.1)

  In this test a memory write and invalidate command with two data phases must be executed by IUT.



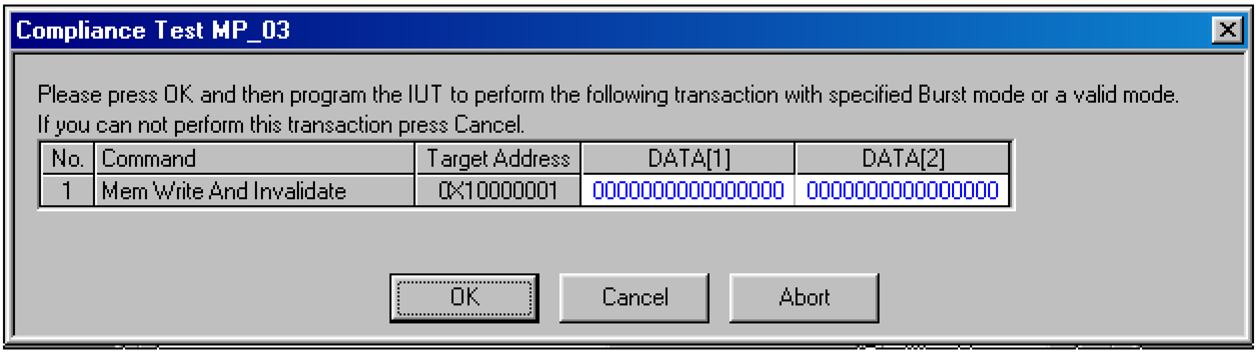
Compliance Test MP_02

Please press OK and then program the IUT to perform the following transaction with BE# = 1100 or a valid Byte Enable.
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write and Invalidate	0X10000000	0000000000000000	0000000000000000

- **MP_03**
  IUT always uses Linear Burst Ordering for Memory Write Invalidate cycles. (3.1.1)

  Like previous test a memory write and invalidate command with two data phases must be executed. The memory address of this test is incremented by one, e.g. 10000001H.



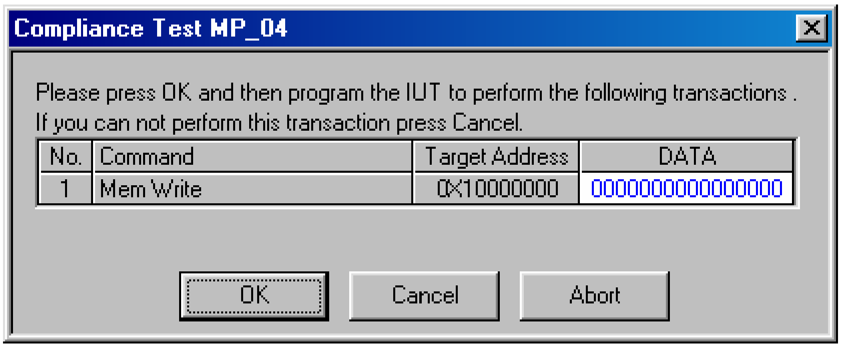
Compliance Test MP_03

Please press OK and then program the IUT to perform the following transaction with specified Burst mode or a valid mode.
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write And Invalidate	0X10000001	0000000000000000	0000000000000000

- **MP_04**
  IUT always drives IRDY# when data is valid during a write transaction. (3.2.1)

  In this test a memory write command with one data phase must be executed by IUT.



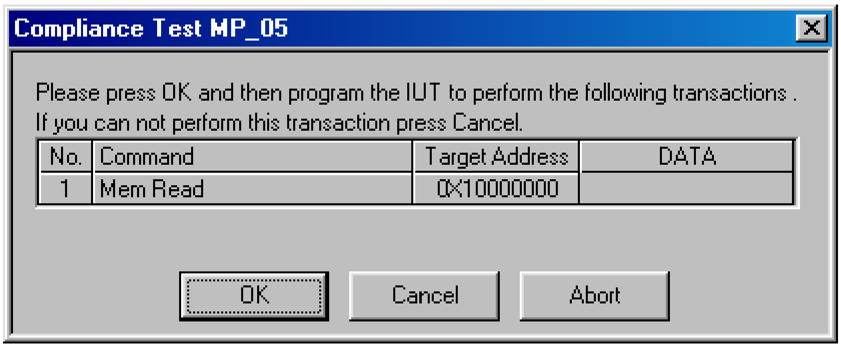
Compliance Test MP_04

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Write	0X10000000	0000000000000000

- **MP_05**
  IUT only transfers data when both IRDY# and TRDY# are asserted on the same rising clock edge. (3.2.1)

  In this test a memory read command with one data phase must be executed by IUT.



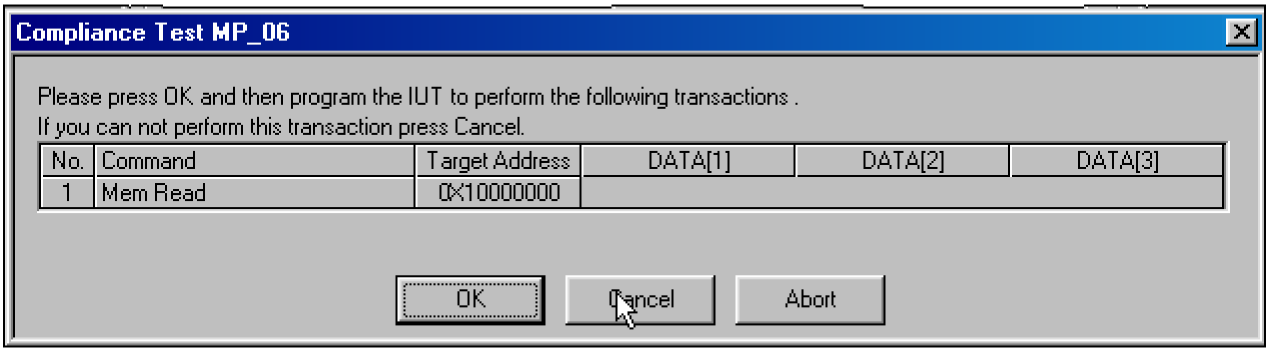
Compliance Test MP_05

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Read	0X10000000	

- **MP_06**
  Once the IUT asserts IRDY# it never changes FRAME# until the current data phase completes. (3.2.1)

  In this test a memory read command with three data phases must be executed by IUT.



Compliance Test MP_06

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

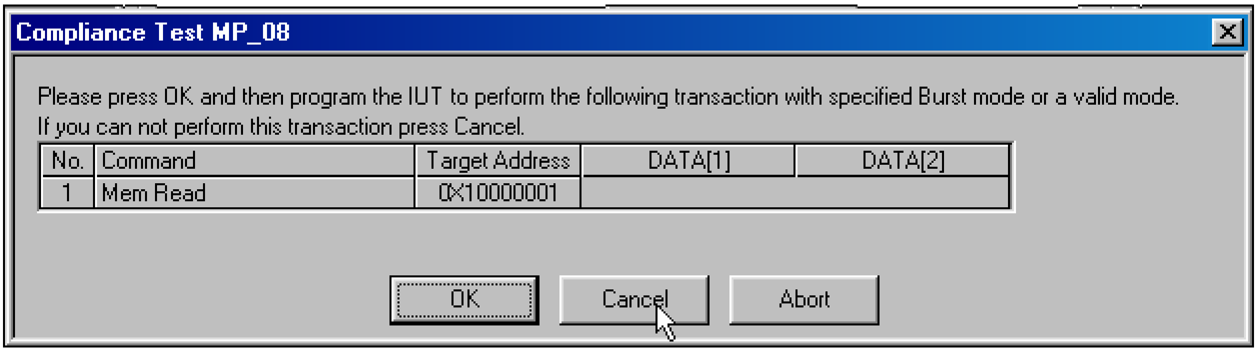
No.	Command	Target Address	DATA[1]	DATA[2]	DATA[3]
1	Mem Read	0X10000000			

- **MP_07**
  Once the IUT asserts IRDY# it never changes IRDY# until the current data phase completes. (3.2.1)

  Part of MP_06 test group.

- **MP_08**
  IUT never uses reserved burst ordering (AD(1:0)=B'01'). (3.2.2)

  In this test a memory read command with two data phases must be executed by IUT. The memory address of this test is incremented by one, e.g. 10000001H.



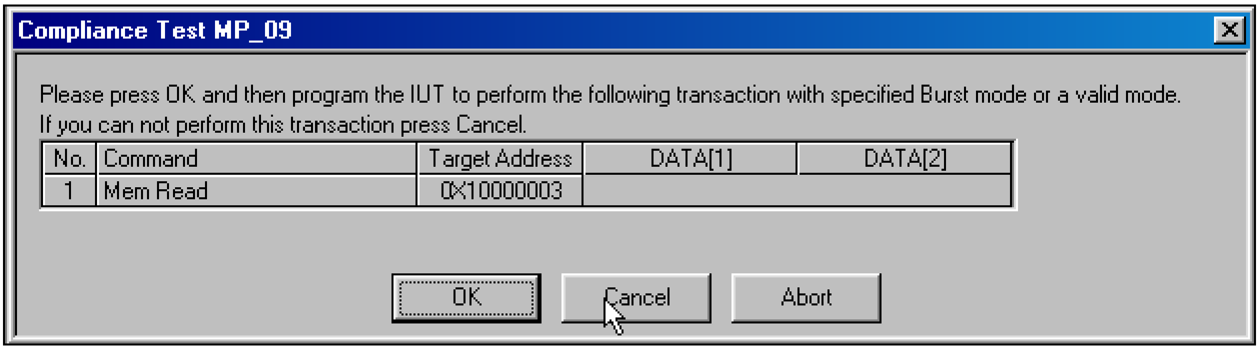
Compliance Test MP_08

Please press OK and then program the IUT to perform the following transaction with specified Burst mode or a valid mode.
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read	0X10000001		

- **MP_09**
  IUT never uses reserved burst ordering (AD(1:0)=B'11'). (3.2.2)

  In this test a memory read command with two data phases must be executed by IUT. The memory address of this test is incremented by three, e.g. 10000003H.



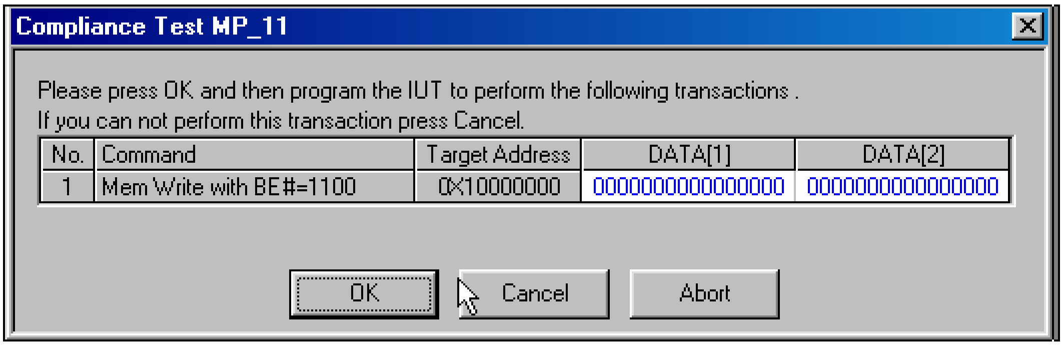
Compliance Test MP_09

Please press OK and then program the IUT to perform the following transaction with specified Burst mode or a valid mode.
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read	0X10000003		

- **MP_11**
  The IUT AD lines are driven to stable values during every address and data phase. (3.2.4)

  In this test a memory write command with two data phases must be executed by IUT. The CBE#[3:0] in the data phases must be 1100B.



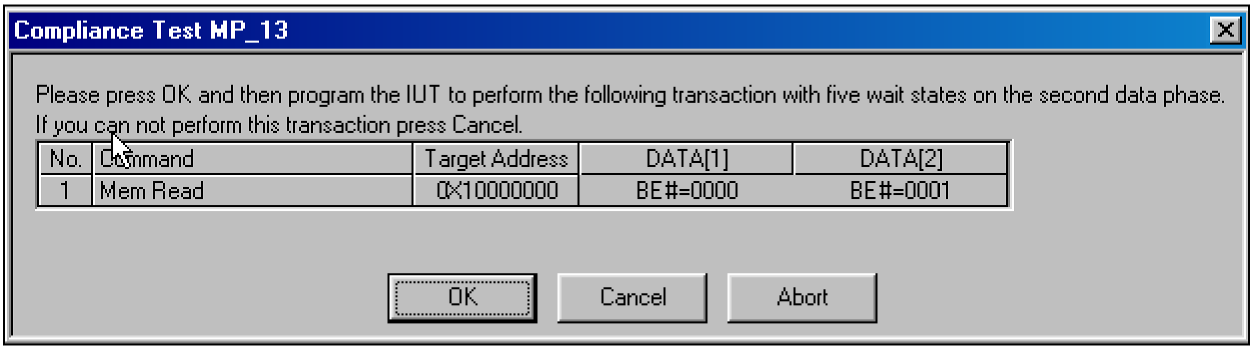
Compliance Test MP_11

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write with BE#=1100	0X10000000	0000000000000000	0000000000000000

- **MP_13**
  The IUT C/BE# lines contain valid Byte Enable information during the entire data phase. (3.31)

  In this test a memory read command with two data phases must be executed by IUT. The CBE#[3:0] of the first data phase must be 0000B and in the second data phase 0001B.



Compliance Test MP_13

Please press OK and then program the IUT to perform the following transaction with five wait states on the second data phase.
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read	0X10000000	BE#=0000	BE#=0001

- **MP_14**
  IUT never de-asserts FRAME# unless IRDY# is asserted or will be asserted. (3.3.3.1)

  Part of MP_06 test group.

- **MP_15**
  IUT never de-asserts IRDY# until at least one clock after FRAME# is de-asserted. (3.3.3.1)

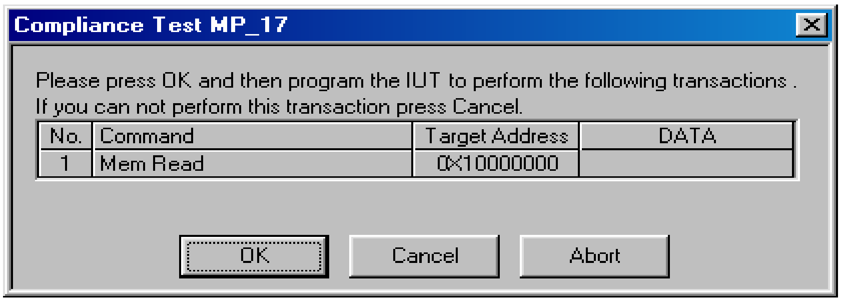
  Part of MP_06 test group.

- **MP_16**
  Once the IUT de-asserts FRAME# it never reasserts FRAME# during the same transaction. (3.3.3.1)

  Part of MP_06 test group.

- **MP_17**
  IUT never terminates with master abort once target has asserted DEVSEL#. (3.3.3.1)

  In this test a memory read command with one data phase must be executed by IUT.



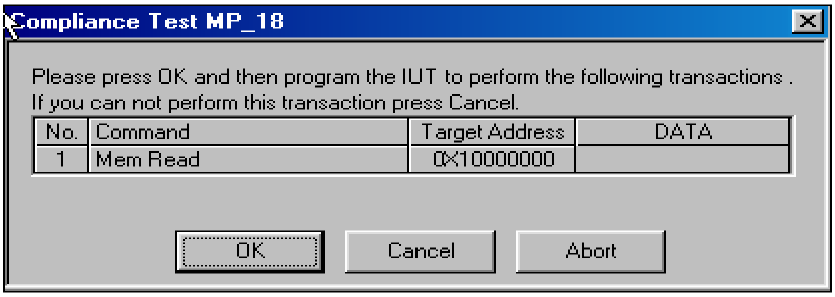
Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Read	0X10000000	

- **MP_18**

  IUT never signals master abort earlier than 5 clocks after FRAME# was first sampled asserted. (3.3.3.1)

  In this test a memory read command with one data phase must be executed by IUT.

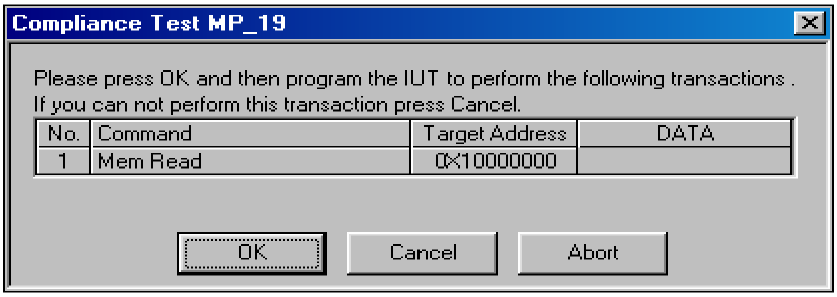


Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Read	0X10000000	

- **MP_19**
  IUT always repeats an access exactly as the original when terminated by retry. (3.3.3.2.2)

  In this test a memory read command with one data phase must be executed by IUT.



Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

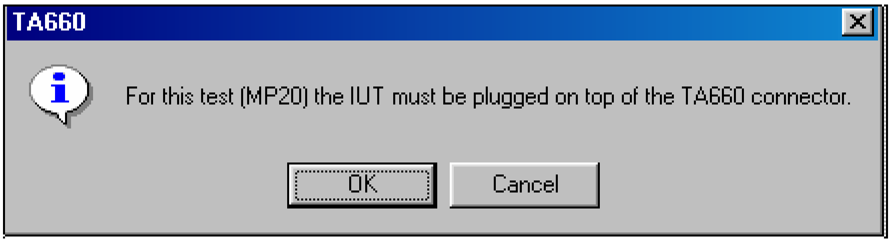
No.	Command	Target Address	DATA
1	Mem Read	0X10000000	

MP_20
IUT never starts cycle unless GNT# is asserted. (3.4.1)

This test requires the IUT to be plugged on top of TA660. Therefore this test can only be done with PCI analyzers and not CPCI. MP_20 will not be executed by the software when user is using TA600C.

Three memory read commands with one data phase for each is requested to check for IUT FRAME# assertion only after GNT# is asserted.

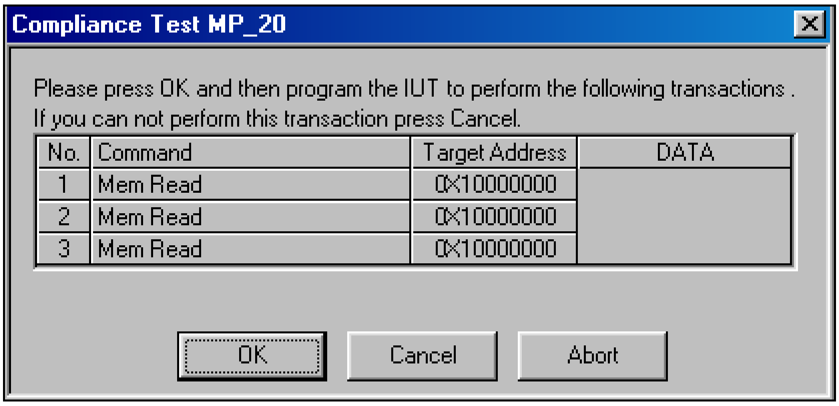
In this test, first the following message is shown:



TA660

For this test (MP20) the IUT must be plugged on top of the TA660 connector.

And then the following message is displayed requesting the data transfer.



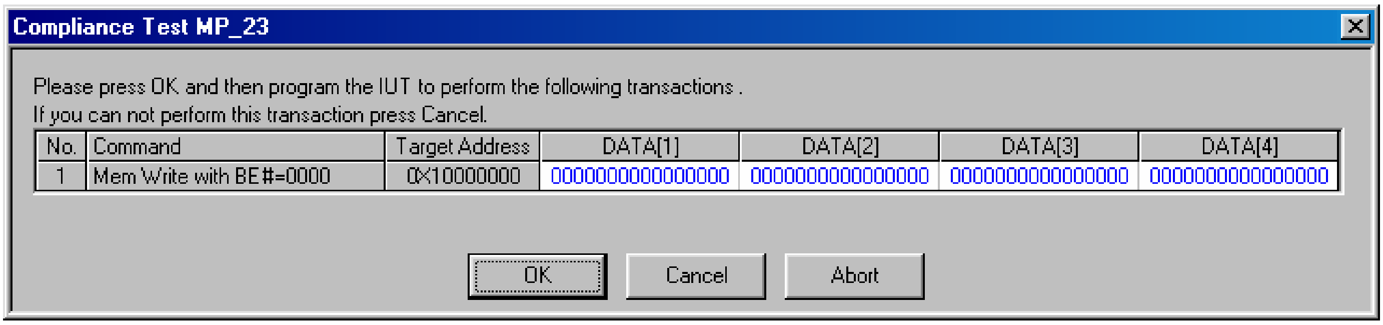
Compliance Test MP_20

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Read	0X10000000	
2	Mem Read	0X10000000	
3	Mem Read	0X10000000	

- **MP_23**
  IUT always asserts IRDY# within eight clocks on all data phases. (3.5.2)

  In this test a memory write command with four data phases must be executed by IUT.



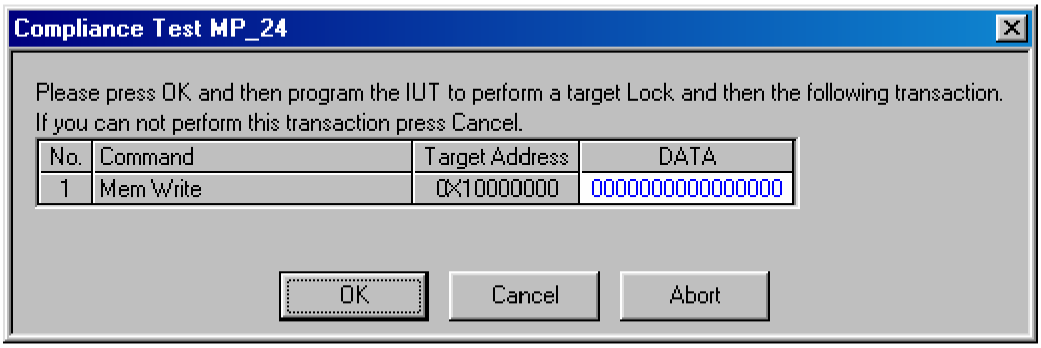
Compliance Test MP_23

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]	DATA[3]	DATA[4]
1	Mem Write with BE#=0000	0X10000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000

- **MP_24**
  IUT always begins lock operation with a read transaction. (3.6)

  In this test a memory write command with one data phase must be executed by IUT.



Compliance Test MP_24

Please press OK and then program the IUT to perform a target Lock and then the following transaction.
If you can not perform this transaction press Cancel.

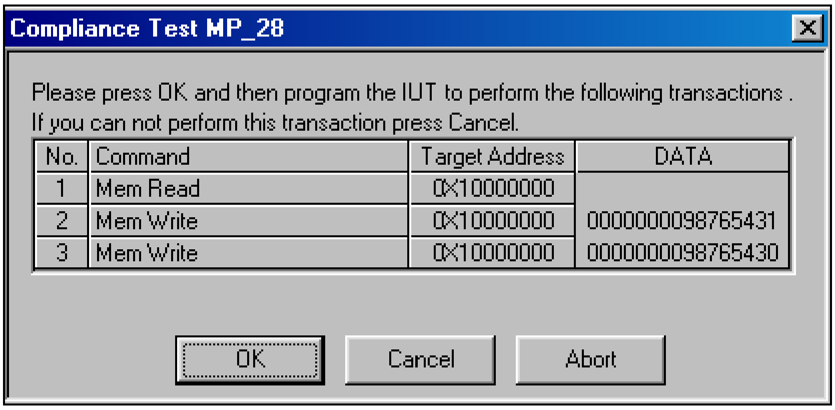
No.	Command	Target Address	DATA
1	Mem Write	0X10000000	0000000000000000

- **MP_25**

  Part of MP_24 test group.

- **MP_28**
  IUT always drives PAR within one clock of C/BE# and AD being driven. (3.8.1)

  In this test three transactions must be executed by IUT all with one data phase. The first transaction is a memory read, the second is a memory write with data equal to 98765431H and the third is a memory write with data equal to 98765430H.



Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

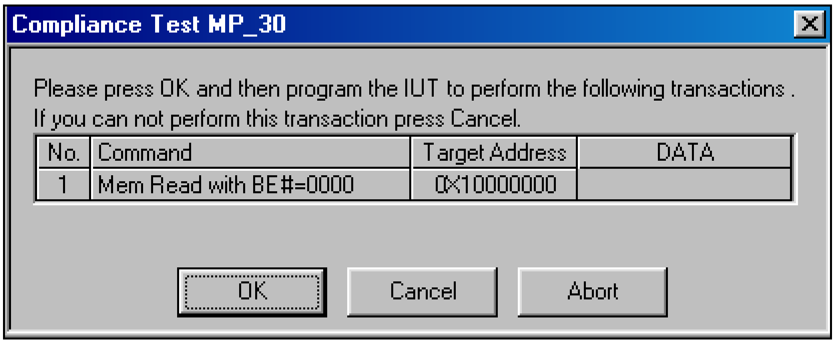
No.	Command	Target Address	DATA
1	Mem Read	0X10000000	
2	Mem Write	0X10000000	0000000098765431
3	Mem Write	0X10000000	0000000098765430

- **MP_29**

  Part of MP_28 test group.

- **MP_30**
  IUT always drives PERR# (when enabled) active two clocks after data when data parity error is detected. (3.8.2.1)

  In this test a memory read command with one data phase must be executed by IUT.

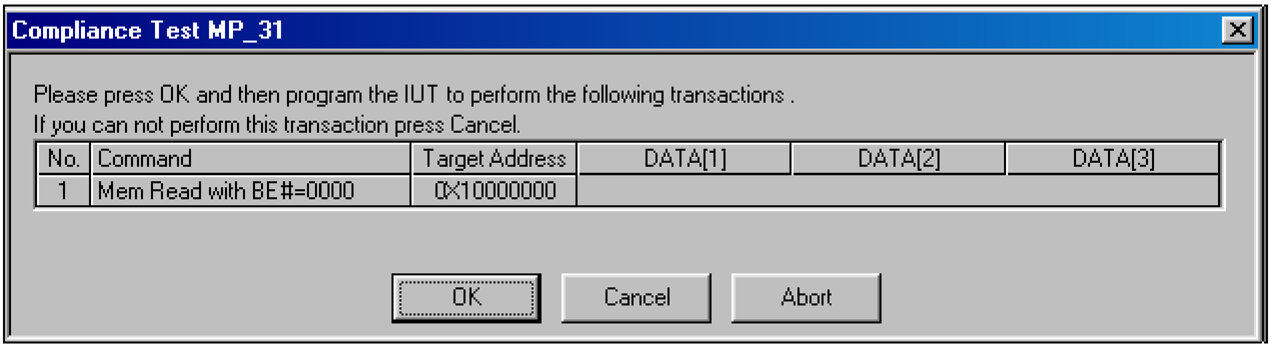


Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Read with BE#=0000	0X10000000	

- **MP_31**
  IUT always drives PERR# (when enabled) for a minimum of 1 clock for each data phase that a parity error is detected. (3.8.2.1)

  In this test a memory read command with three data phases must be executed by IUT.



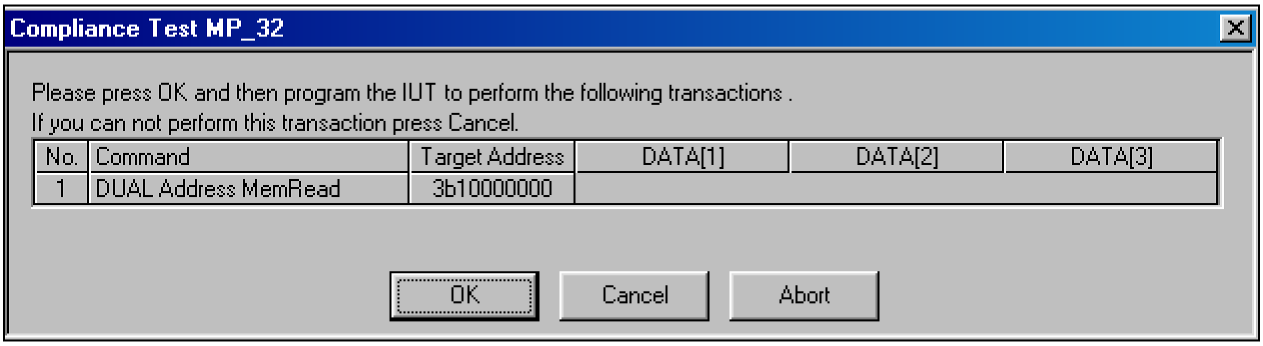
Compliance Test MP_31

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]	DATA[3]
1	Mem Read with BE#=0000	0X10000000			

- **MP_32**
  IUT always holds FRAME# asserted for cycle following DUAL command. (3.10.1)

  In this test dual address cycle is tested thus the address size must be 64-bit. The low 32-bit is the free memory address found by TA660 and the high 32-bit is the constant value 0000003bH. The requested transaction has one data phase.



Compliance Test MP_32

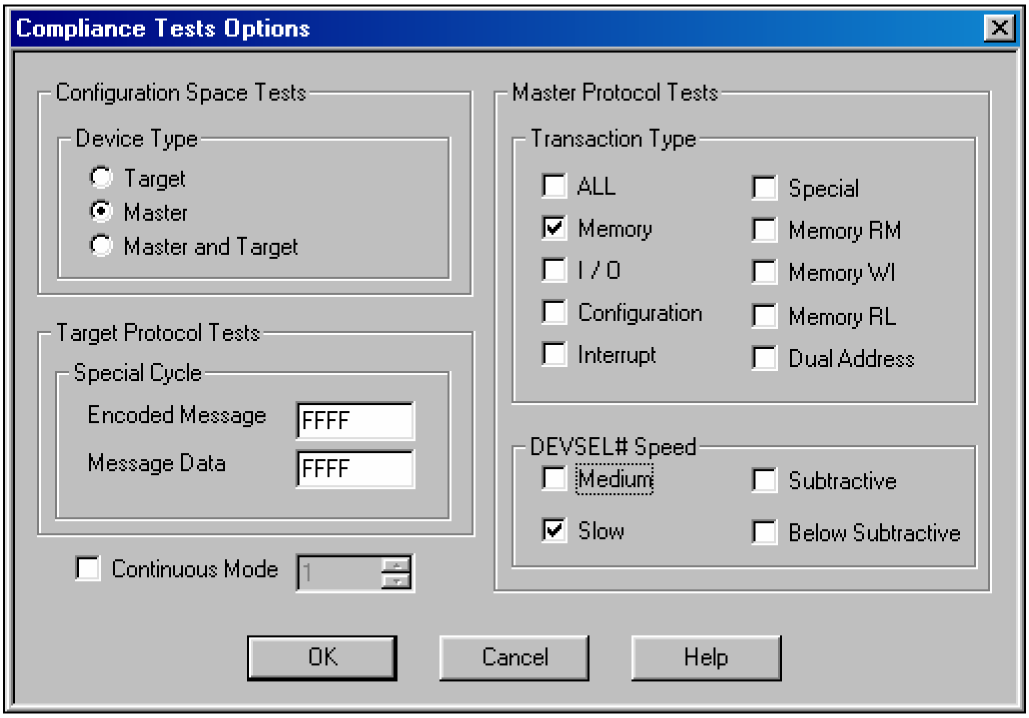
Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]	DATA[3]
1	DUAL Address MemRead	3b10000000			

Component Protocol checklist for a master device

1.01 Tests

It is highly recommended that at the beginning the users select only one "Transaction Type" and one "DEVSEL# Speed" to be sure they can execute all the steps correctly and efficiently before enabling more Transaction Types. In some cases each added Transaction adds about 16 tests.



Compliance Tests Options

Configuration Space Tests

Device Type
○ Target
● Master
○ Master and Target

Target Protocol Tests

Special Cycle
Encoded Message FFFF
Message Data FFFF

□ Continuous Mode 1

Master Protocol Tests

Transaction Type
□ ALL
☑ Memory
□ I / O
□ Configuration
□ Interrupt
□ Special
□ Memory RM
□ Memory WI
□ Memory RL
□ Dual Address

DEVSEL# Speed
□ Medium
☑ Slow
□ Subtractive
□ Below Subtractive

Please note that not all devices are designed to perform all transactions, the user is expected to be familiar with the specification of the device and enable only the appropriate tests.

There are four sets of transactions that may be executed in these tests, if all the selections have been made in the options. Otherwise only the selected categories will be tested.

The first set is a memory read command followed by a memory write command both with one or more data phases.

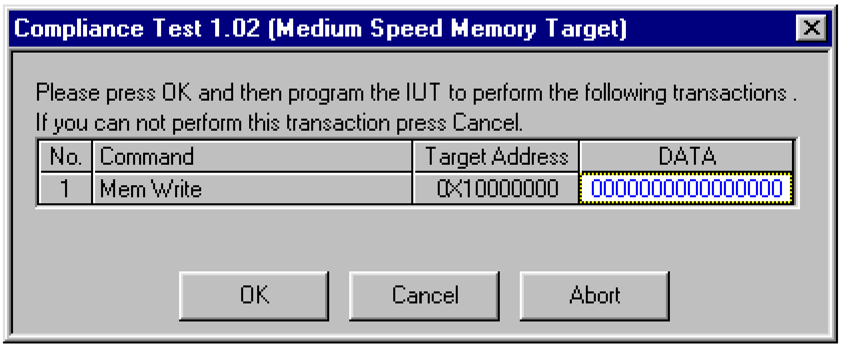
The second set is an I/O read followed by an I/O write command both with one or more data phases.

The third set is a configuration read followed by a configuration write command both with one or more data phases.

The last set includes some single commands. These commands are:

1. Memory Read Multiple
2. Memory Read Line
3. Memory Write & Invalidate
4. Special Cycle

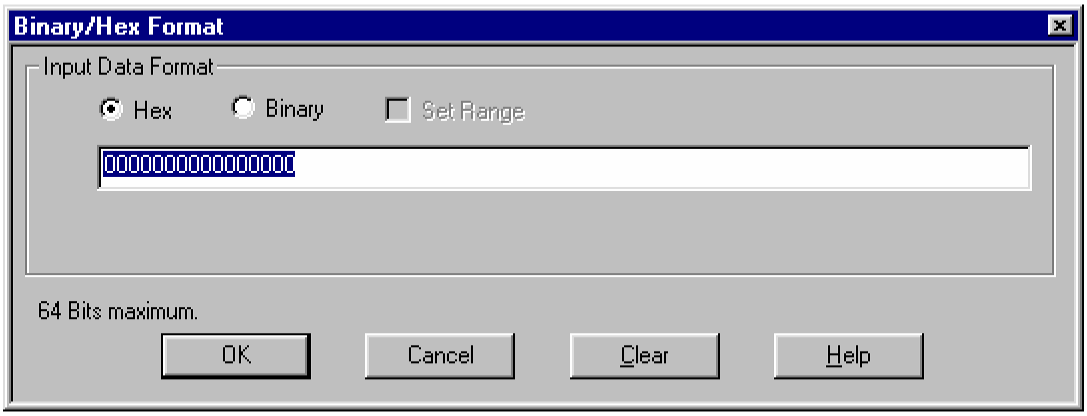
The first three commands may have one or more data phases.
In all sets the data to be written by IUT can be changed. For example user may write 12345678H in the memory write command of test 1.02 by selecting the data field and changing the data.



Compliance Test 1.02 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Write	0X10000000	0000000000000000



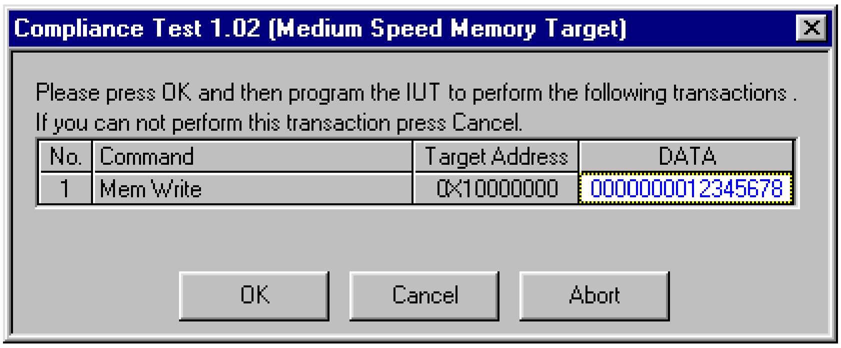
Binary/Hex Format

Input Data Format

● Hex ○ Binary □ Set Range

0000000000000000

64 Bits maximum.



Compliance Test 1.02 (Medium Speed Memory Target)

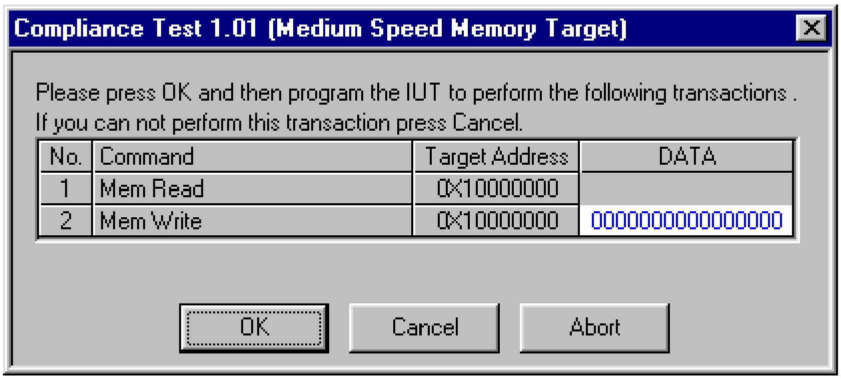
Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Write	0X10000000	0000000012345678

- **1.01**

PCI DEVICE SPEED (AS INDICATED BY DEVSEL#) TEST

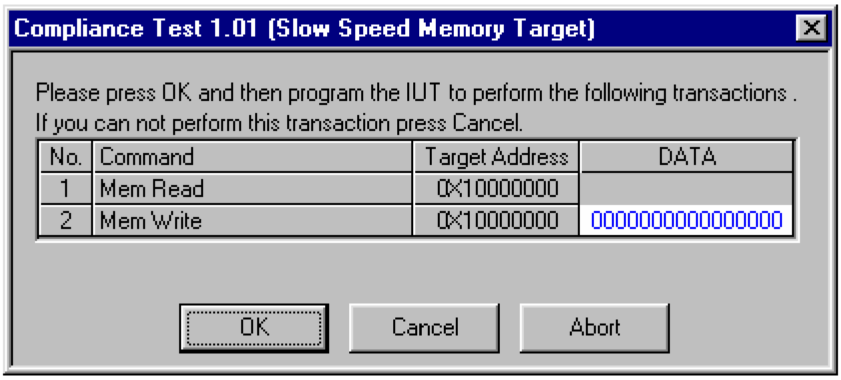
There are four sets of transactions that must be executed in this test. The first set is a memory read command followed by a memory write command both with one data phase, this set is repeated four times. Then the second set is an I/O read followed by an I/O write command both with one data phase, this set is repeated two times on active motherboards (like computer systems) or four times on passive boards because. Please note on active boards the tests for subtractive and below subtractive I/O target speed can not be executed since the processor or the bridge may respond. The third set is a configuration read followed by a configuration write command both with one data phase. This set is repeated four times. The last section is a special cycle command which is not repeated.



Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Read	0X10000000	
2	Mem Write	0X10000000	0000000000000000

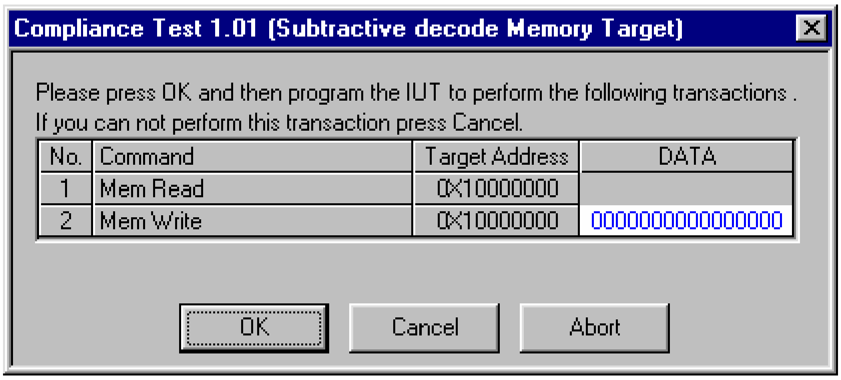
Medium Speed Memory



Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Read	0X10000000	
2	Mem Write	0X10000000	0000000000000000

Slow Speed Memory

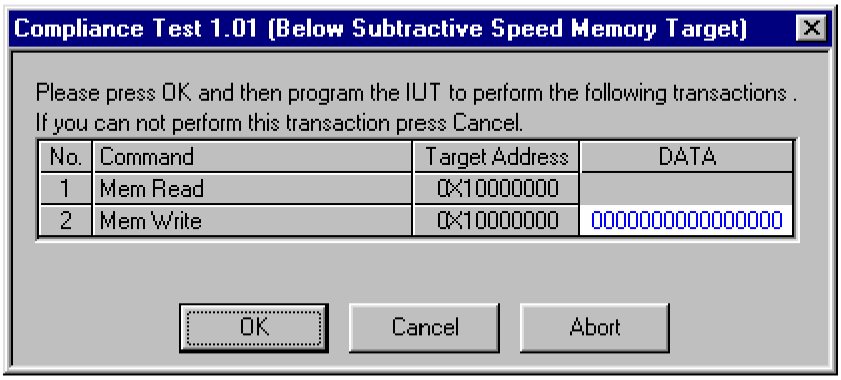


Compliance Test 1.01 (Subtractive decode Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Read	0X10000000	
2	Mem Write	0X10000000	0000000000000000

Subtractive Speed Memory

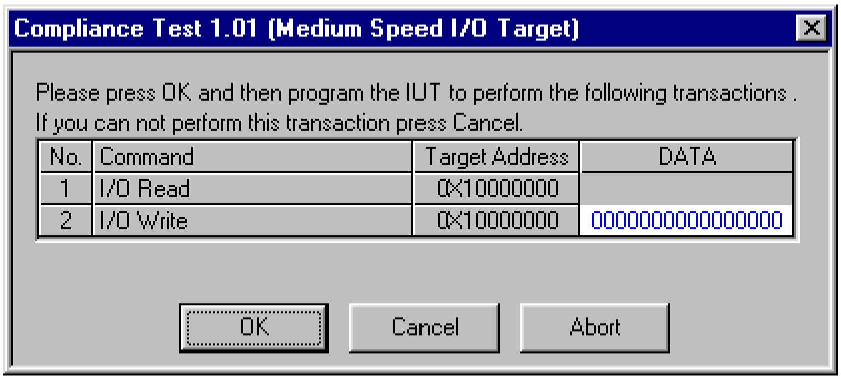


Compliance Test 1.01 (Below Subtractive Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Read	0X10000000	
2	Mem Write	0X10000000	0000000000000000

Below Subtractive Speed Memory

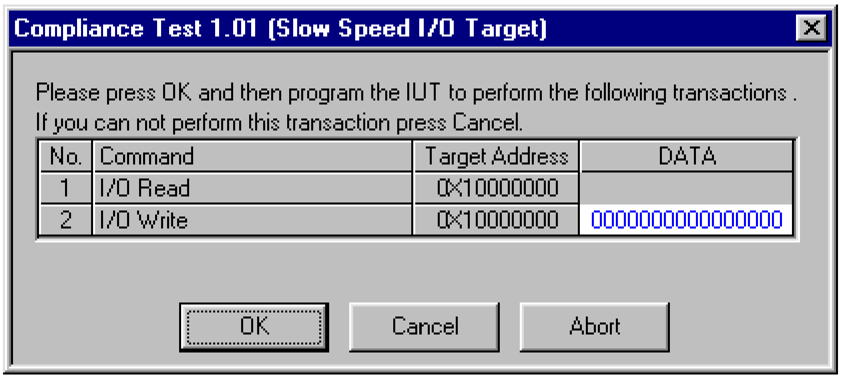


Compliance Test 1.01 (Medium Speed I/O Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	I/O Read	0X10000000	
2	I/O Write	0X10000000	0000000000000000

Medium Speed I/O

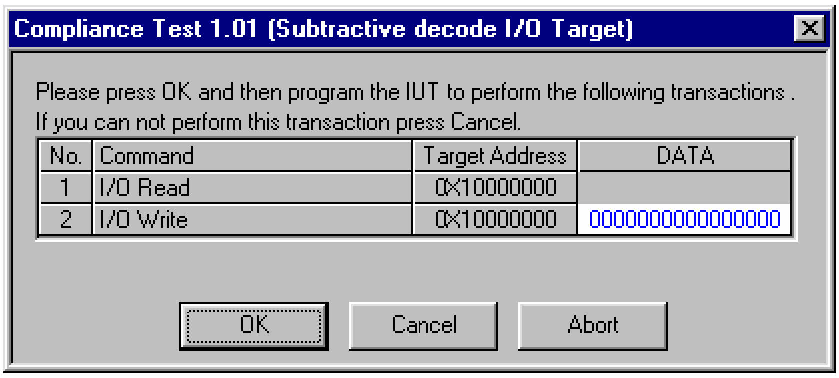


Compliance Test 1.01 (Slow Speed I/O Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	I/O Read	0X10000000	
2	I/O Write	0X10000000	0000000000000000

Slow Speed I/O

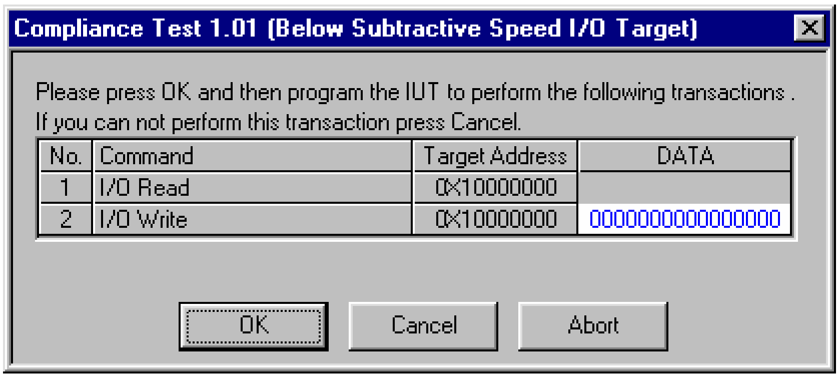


Compliance Test 1.01 (Subtractive decode I/O Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	I/O Read	0X10000000	
2	I/O Write	0X10000000	0000000000000000

Subtractive Speed I/O

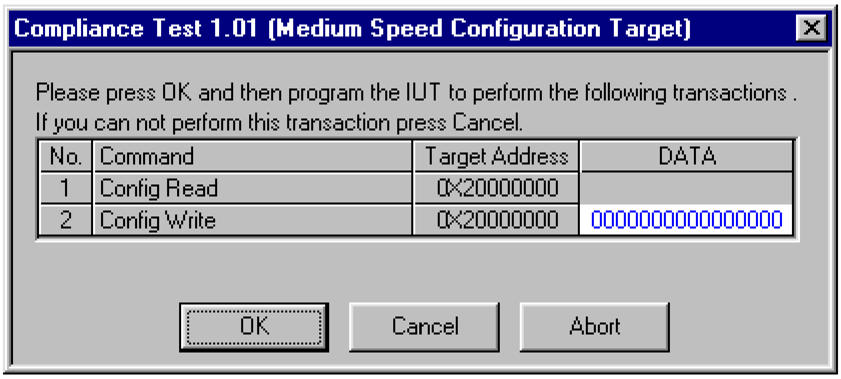


Compliance Test 1.01 (Below Subtractive Speed I/O Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	I/O Read	0X10000000	
2	I/O Write	0X10000000	0000000000000000

Below Subtractive Speed I/O

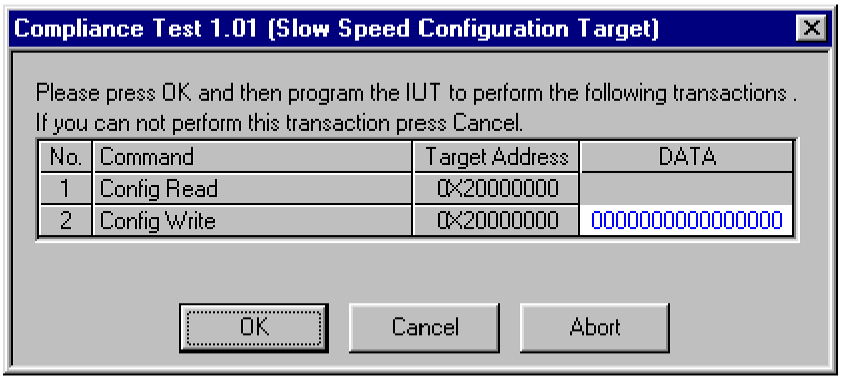


Compliance Test 1.01 (Medium Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Config Read	0X20000000	
2	Config Write	0X20000000	0000000000000000

Medium Speed Configuration

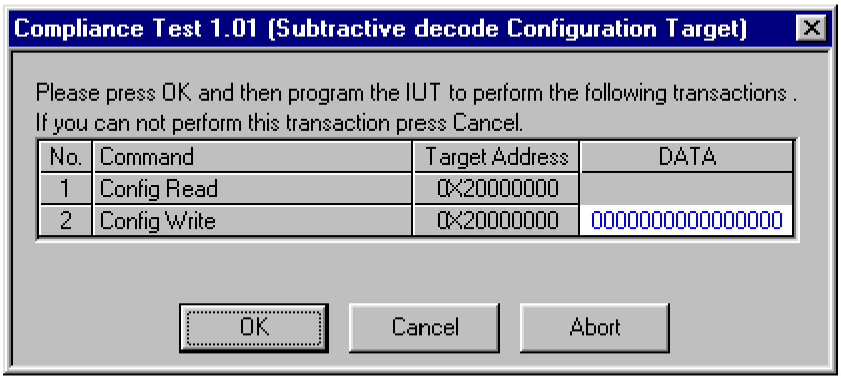


Compliance Test 1.01 (Slow Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Config Read	0X20000000	
2	Config Write	0X20000000	0000000000000000

Slow Speed Configuration

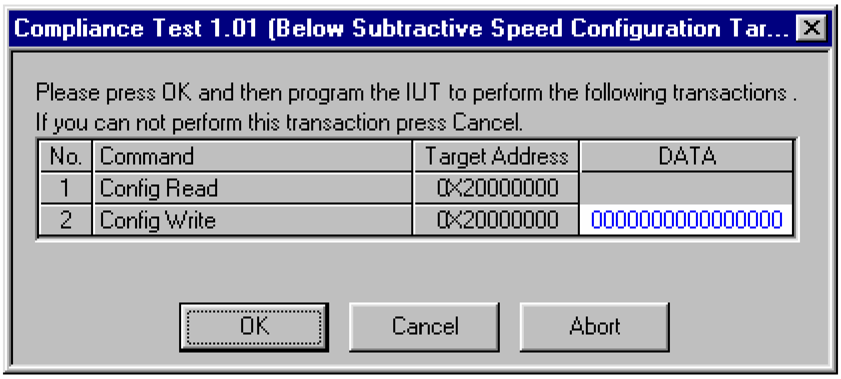


Compliance Test 1.01 (Subtractive decode Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Config Read	0X20000000	
2	Config Write	0X20000000	0000000000000000

Subtractive Speed Configuration

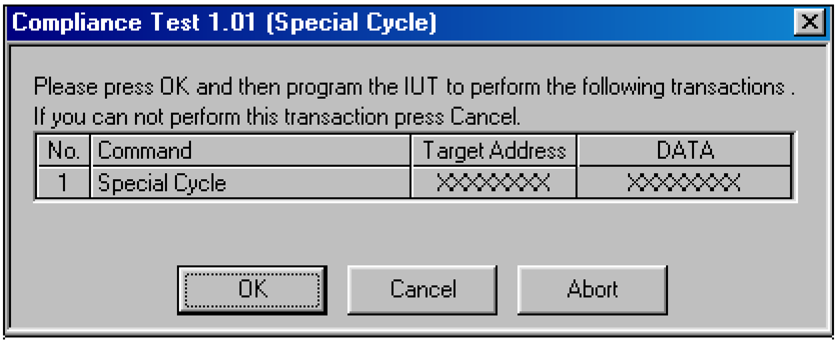


Compliance Test 1.01 (Below Subtractive Speed Configuration Tar...

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Config Read	0X20000000	
2	Config Write	0X20000000	0000000000000000

Below Subtractive Speed Configuration



Compliance Test 1.01 (Special Cycle)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

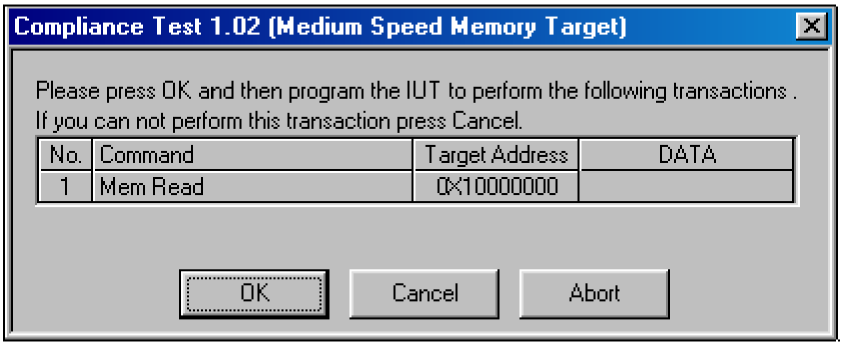
No.	Command	Target Address	DATA
1	Special Cycle	XXXXXXXX	XXXXXXXX

Special Cycle Test

- **1.02**

PCI BUS SINGLE DATA PHASE TARGET ABORT CYCLES

The transactions of this section are similar to the previous section (1.01) with the exception that the memory and configuration sets are repeated three times instead of four, the I/O set is repeated two times on active boards and three times on passive boards and the special cycle is not needed.

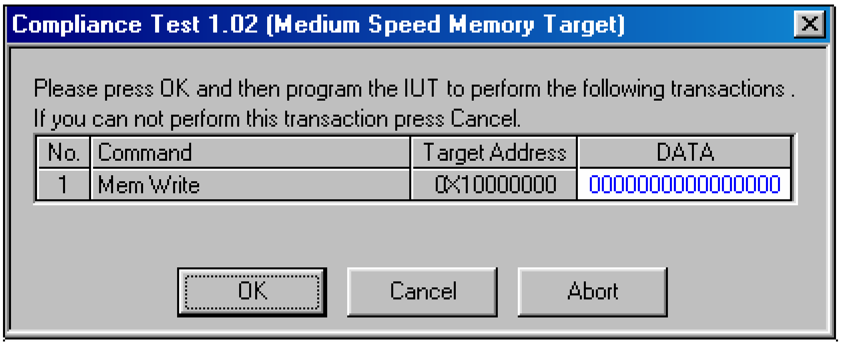


Compliance Test 1.02 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Read	0X10000000	

Medium Speed Memory Read

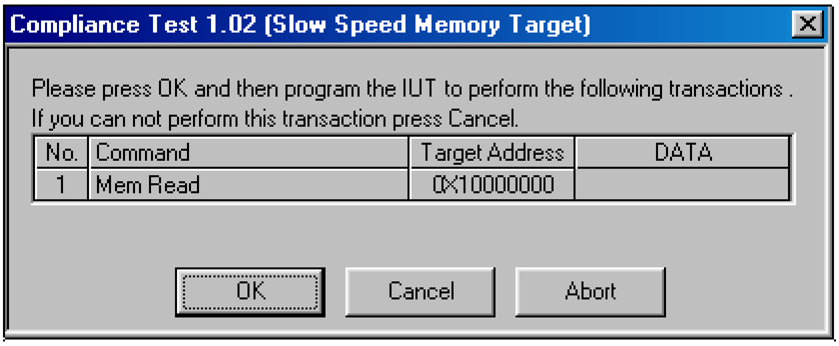


Compliance Test 1.02 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Write	0X10000000	0000000000000000

Medium Speed Memory Write

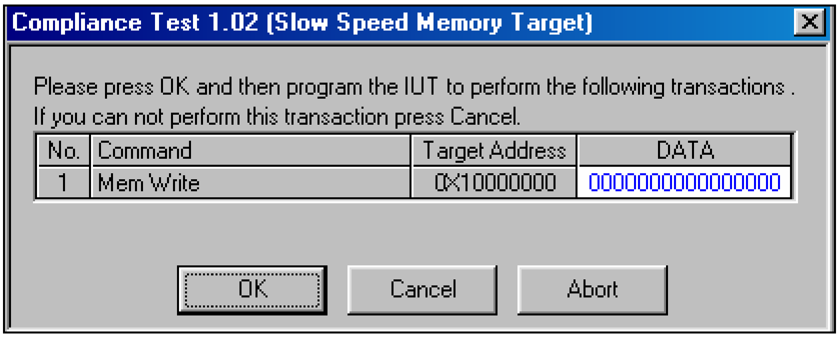


Compliance Test 1.02 (Slow Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Read	0X10000000	

Slow Speed Memory Read

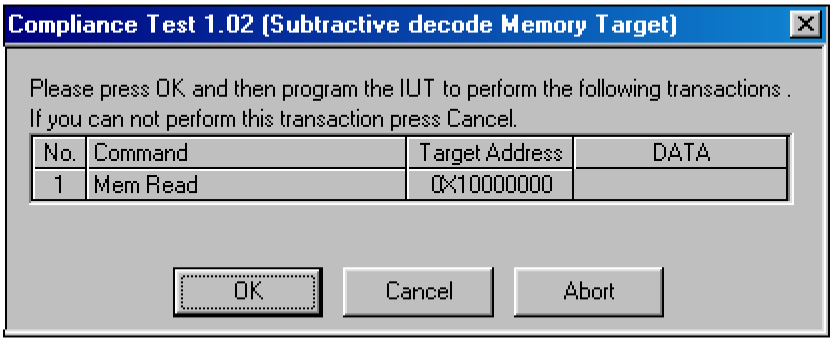


Compliance Test 1.02 (Slow Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Write	0X10000000	0000000000000000

Slow Speed Memory Write

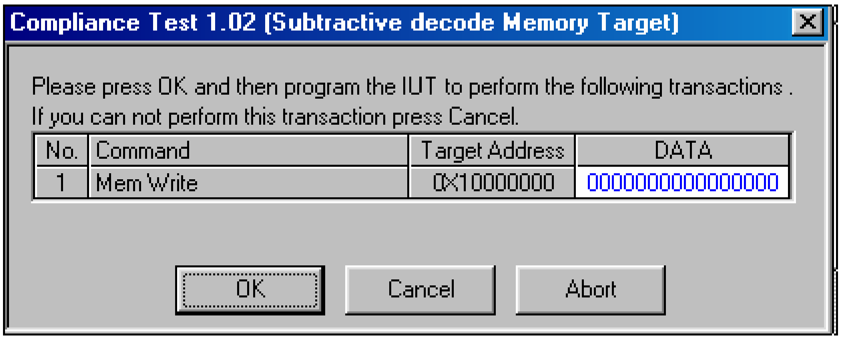


Compliance Test 1.02 (Subtractive decode Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Read	0X10000000	

Subtractive Speed Memory Read

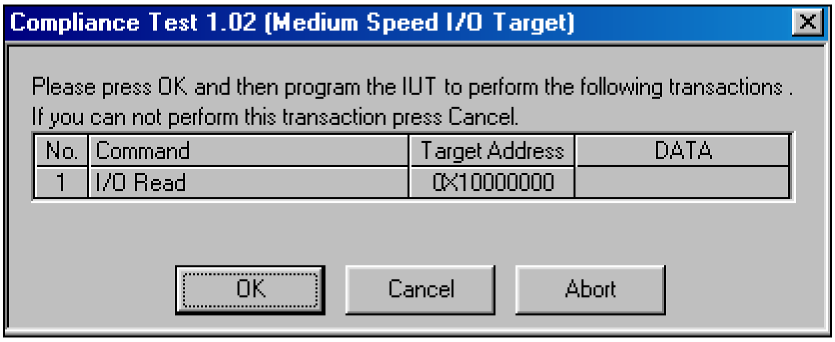


Compliance Test 1.02 (Subtractive decode Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Mem Write	0X10000000	0000000000000000

Subtractive Speed Memory Write

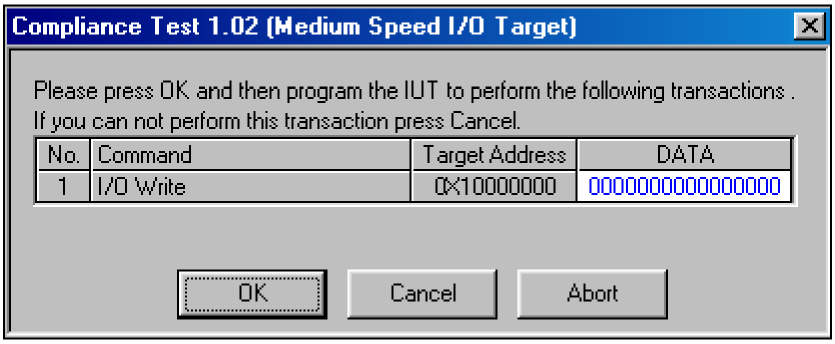


Compliance Test 1.02 (Medium Speed I/O Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	I/O Read	0X10000000	

Medium Speed I/O Read

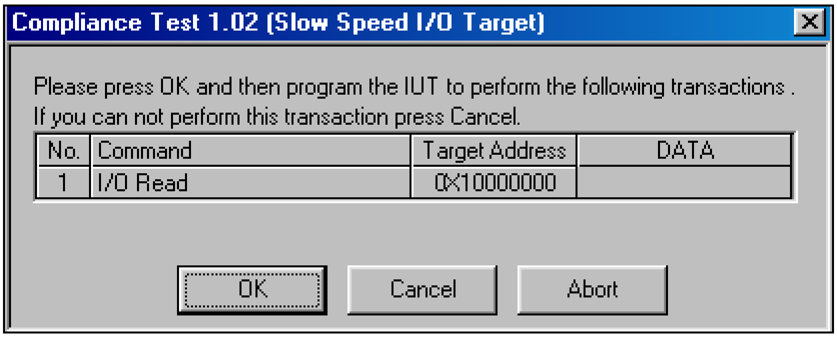


Compliance Test 1.02 (Medium Speed I/O Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	I/O Write	0X10000000	0000000000000000

Medium Speed I/O Write

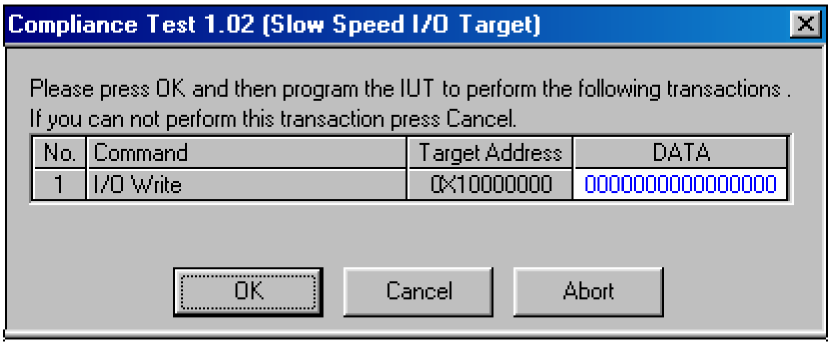


Compliance Test 1.02 (Slow Speed I/O Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	I/O Read	0X10000000	

Slow Speed I/O Read

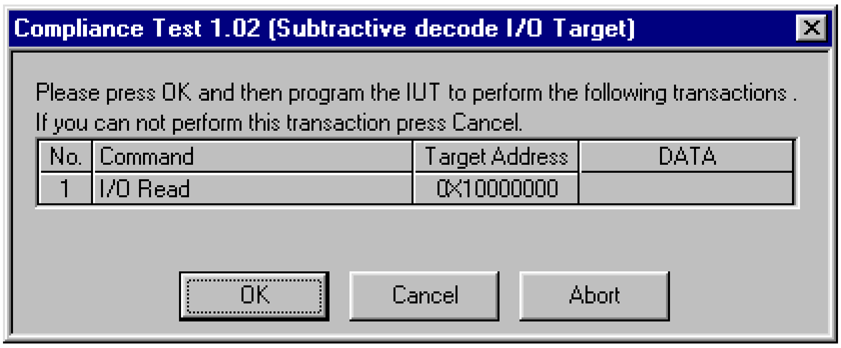


Compliance Test 1.02 (Slow Speed I/O Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	I/O Write	0X10000000	0000000000000000

Slow Speed I/O Write

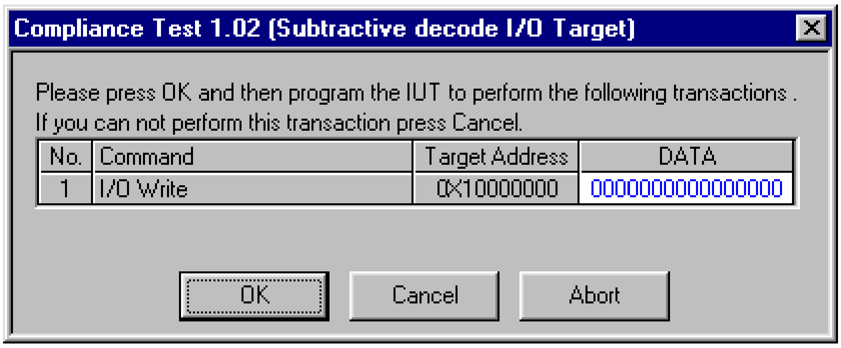


Compliance Test 1.02 (Subtractive decode I/O Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	I/O Read	0X10000000	

Subtractive Speed I/O Read

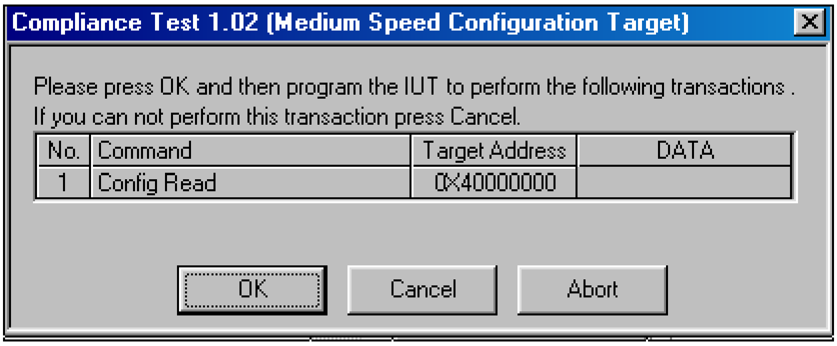


Compliance Test 1.02 (Subtractive decode I/O Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	I/O Write	0X10000000	0000000000000000

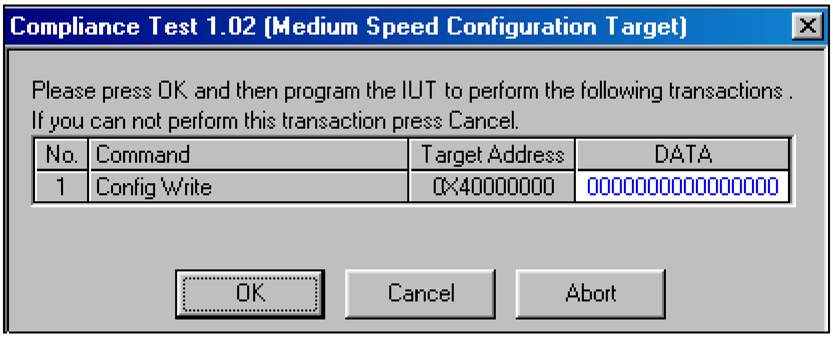
Subtractive Speed I/O Write



Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Config Read	0X40000000	

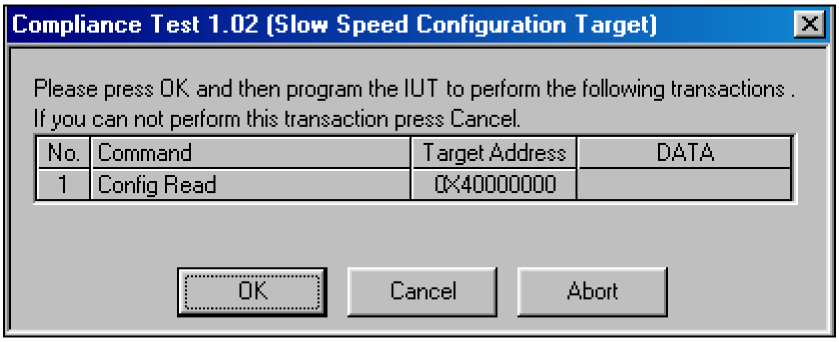
Medium Speed Configuration Read



Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Config Write	0X40000000	0000000000000000

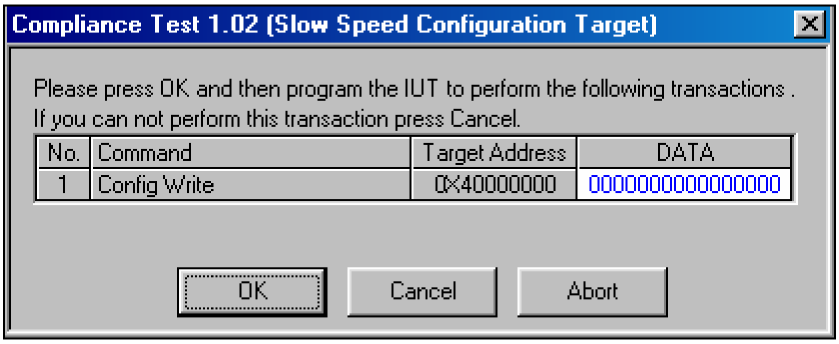
Medium Speed Configuration Write



Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Config Read	0X40000000	

Slow Speed Configuration Read

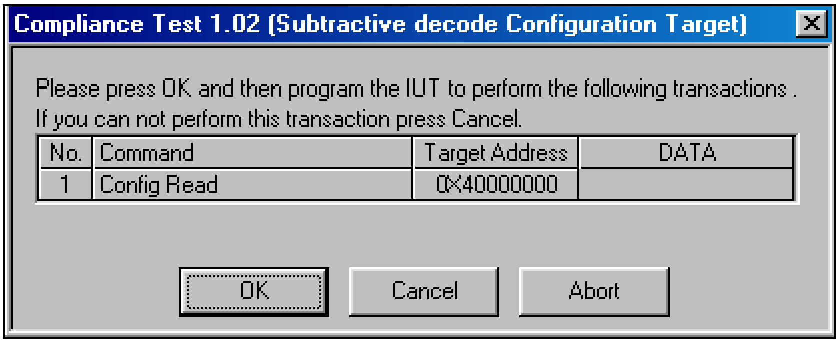


Compliance Test 1.02 (Slow Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Config Write	0X40000000	0000000000000000

Slow Speed Configuration Write

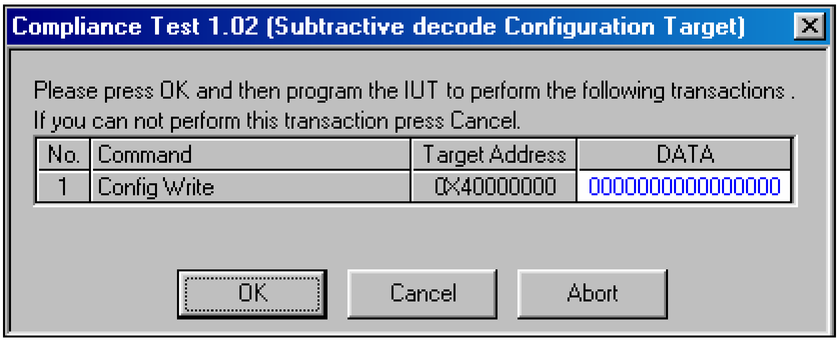


Compliance Test 1.02 (Subtractive decode Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Config Read	0X40000000	

Subtractive Speed Configuration Read



Compliance Test 1.02 (Subtractive decode Configuration Target)

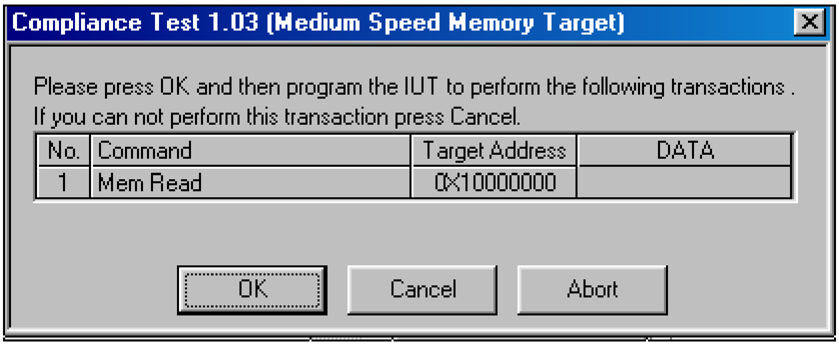
Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Config Write	0X40000000	0000000000000000

Subtractive Speed Configuration Write

- **1.03**
  PCI BUS SINGLE DATA PHASE RETRY CYCLES

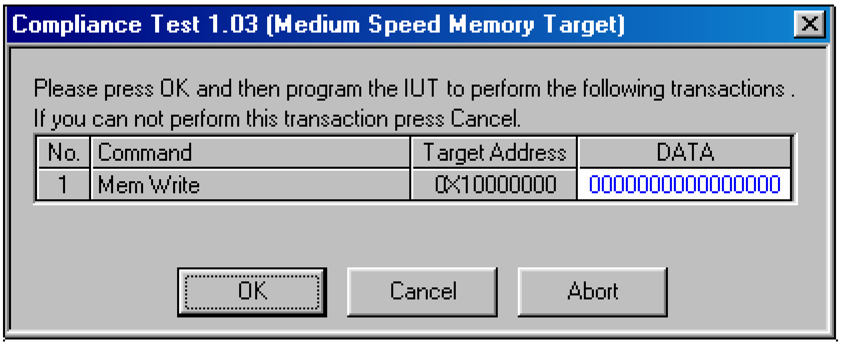
  The transactions of this section are similar to the previous section (1.02) with the exception that sometimes a confirmation message is shown. The software will test for master retry.



Compliance Test 1.03 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

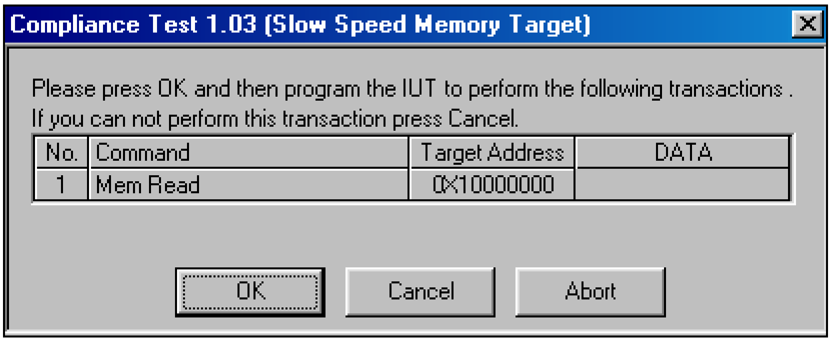
No.	Command	Target Address	DATA
1	Mem Read	0X10000000	



Compliance Test 1.03 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

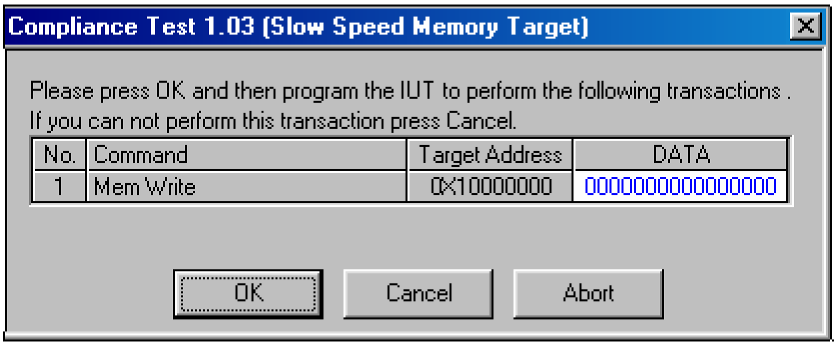
No.	Command	Target Address	DATA
1	Mem Write	0X10000000	0000000000000000



Compliance Test 1.03 (Slow Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

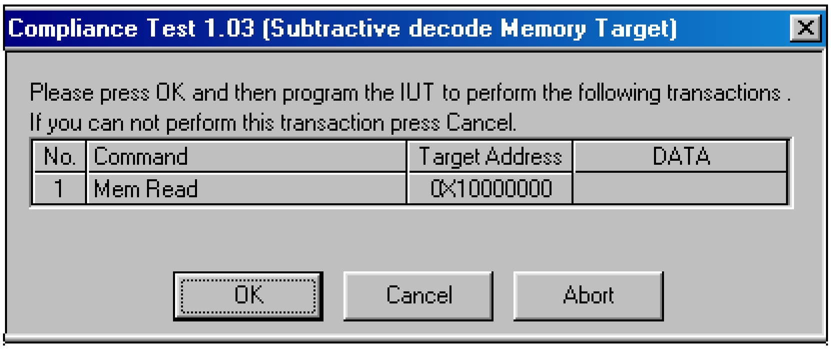
No.	Command	Target Address	DATA
1	Mem Read	0X10000000	



Compliance Test 1.03 (Slow Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

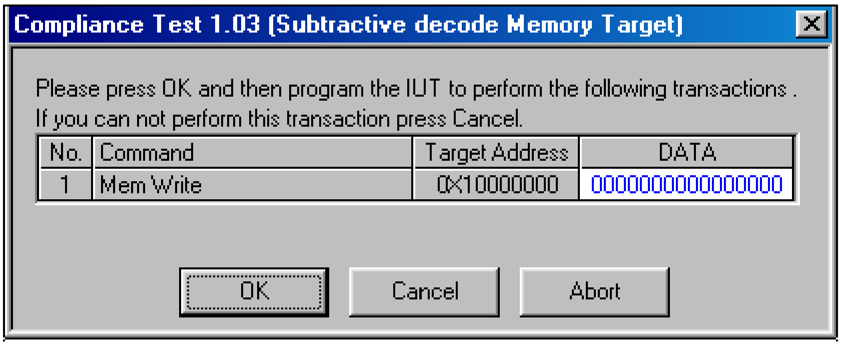
No.	Command	Target Address	DATA
1	Mem Write	0X10000000	0000000000000000



Compliance Test 1.03 (Subtractive decode Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

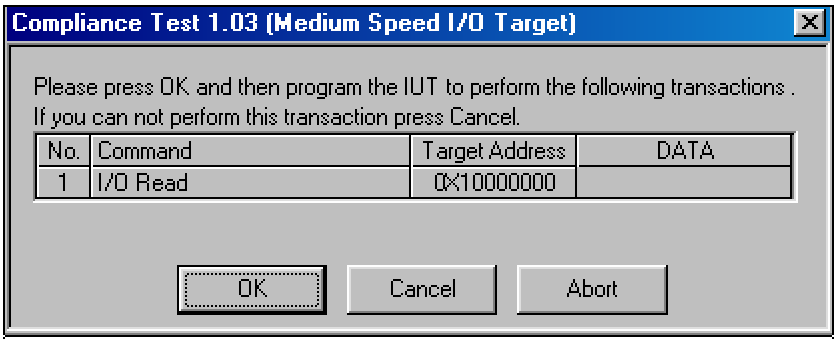
No.	Command	Target Address	DATA
1	Mem Read	0X10000000	



Compliance Test 1.03 (Subtractive decode Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

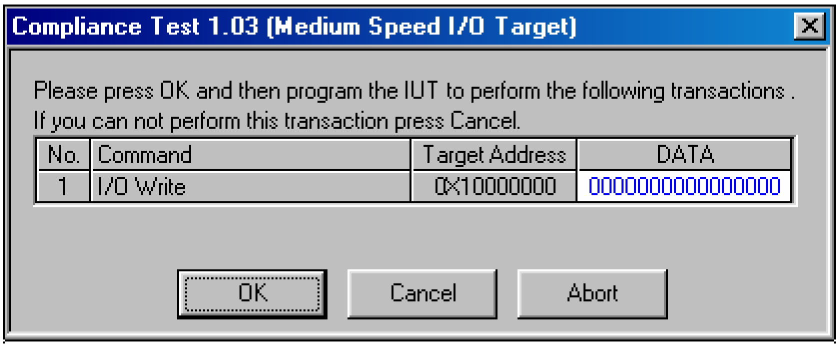
No.	Command	Target Address	DATA
1	Mem Write	0X10000000	0000000000000000



Compliance Test 1.03 (Medium Speed I/O Target)

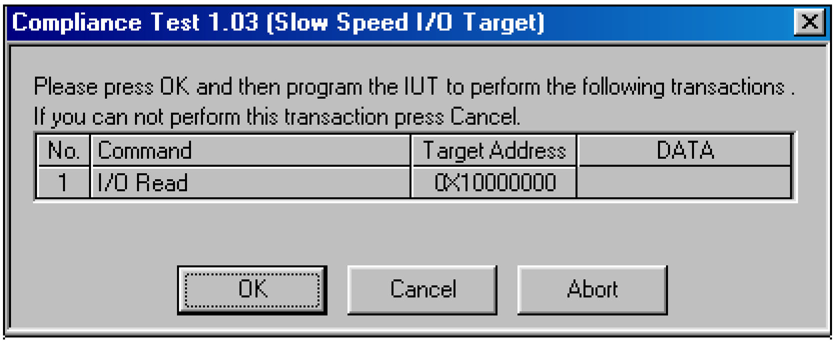
Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	I/O Read	0X10000000	


Compliance Test 1.03 (Medium Speed I/O Target)

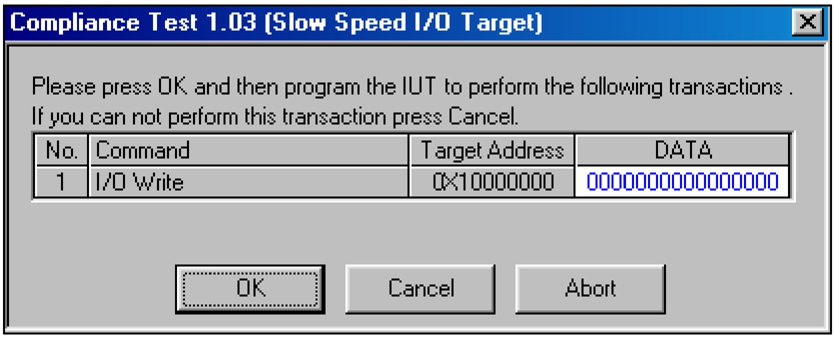
Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	I/O Write	0X10000000	0000000000000000


Compliance Test 1.03 (Slow Speed I/O Target)

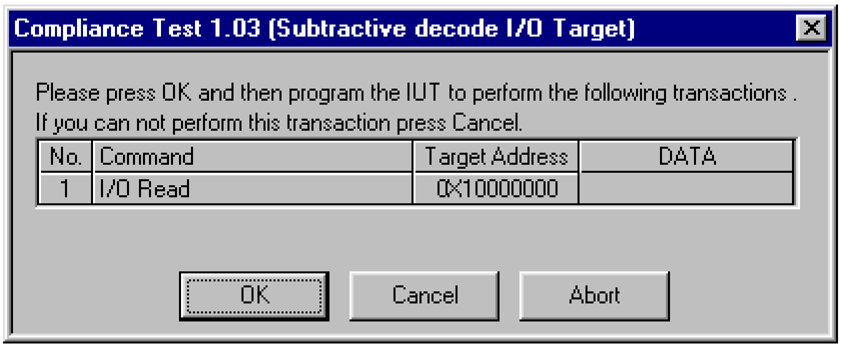
Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	I/O Read	0X10000000	


Compliance Test 1.03 (Slow Speed I/O Target)

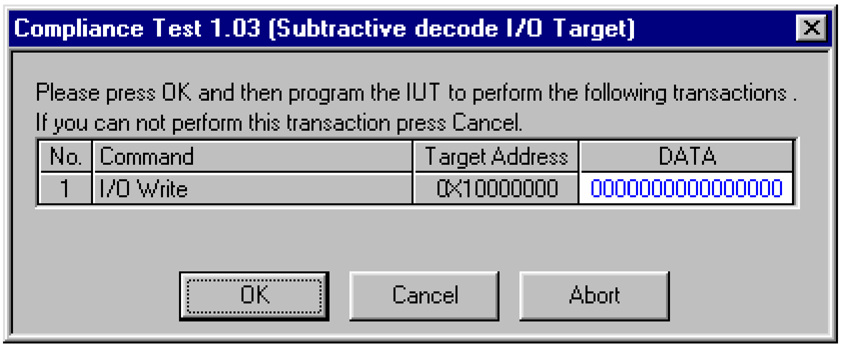
Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	I/O Write	0X10000000	0000000000000000


Compliance Test 1.03 (Subtractive decode I/O Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

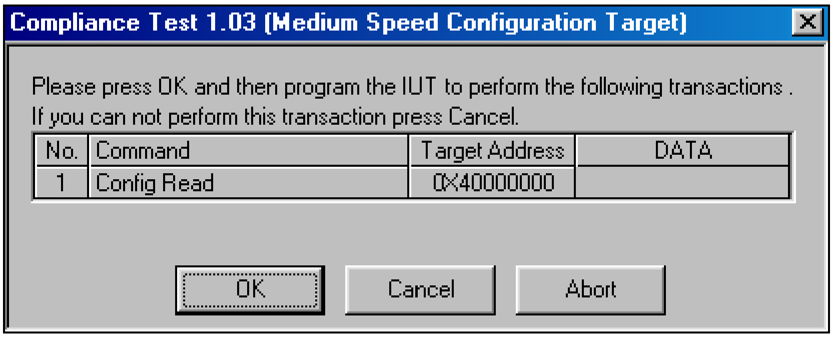
No.	Command	Target Address	DATA
1	I/O Read	0X10000000	



Compliance Test 1.03 (Subtractive decode I/O Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

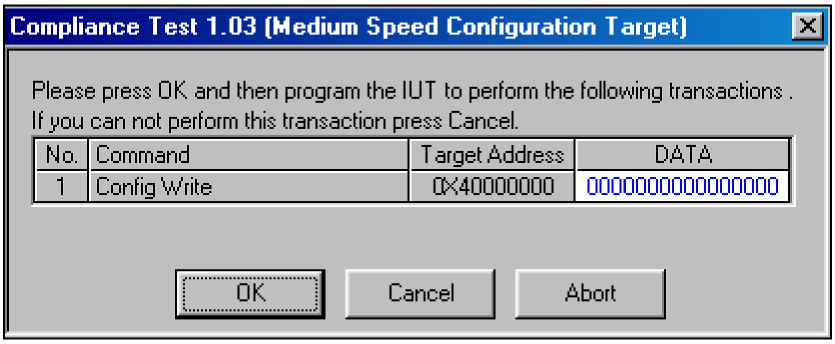
No.	Command	Target Address	DATA
1	I/O Write	0X10000000	0000000000000000



Compliance Test 1.03 (Medium Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

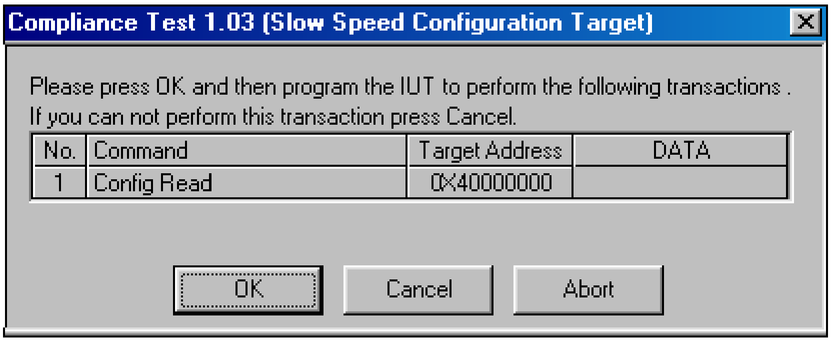
No.	Command	Target Address	DATA
1	Config Read	0X40000000	



Compliance Test 1.03 (Medium Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

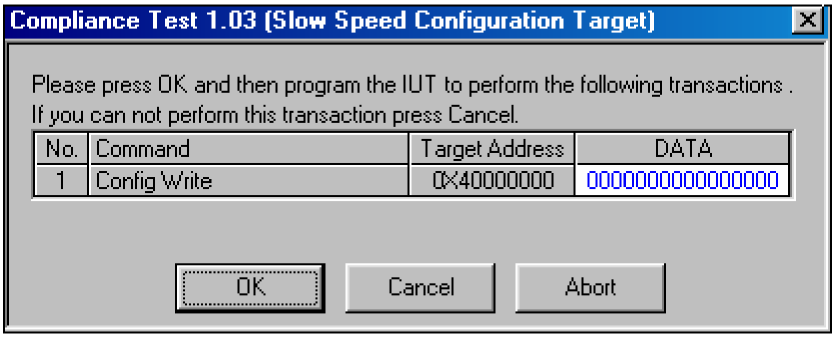
No.	Command	Target Address	DATA
1	Config Write	0X40000000	0000000000000000



Compliance Test 1.03 (Slow Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

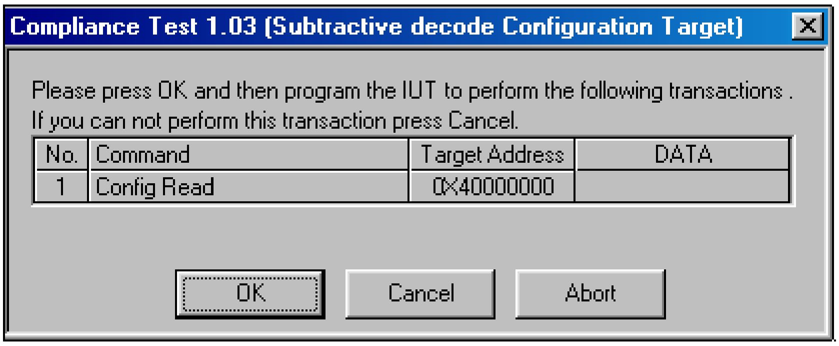
No.	Command	Target Address	DATA
1	Config Read	0X40000000	



Compliance Test 1.03 (Slow Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

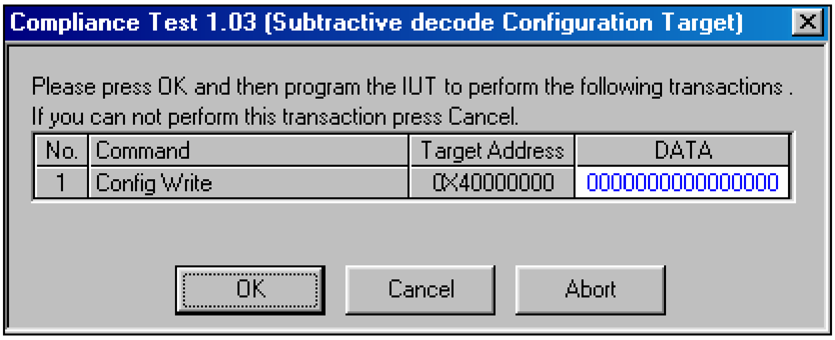
No.	Command	Target Address	DATA
1	Config Write	0X40000000	0000000000000000



Compliance Test 1.03 (Subtractive decode Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Config Read	0X40000000	



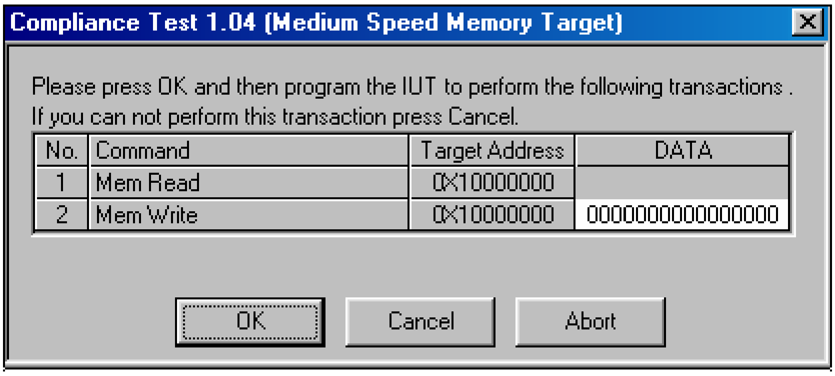
Compliance Test 1.03 (Subtractive decode Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Config Write	0X40000000	0000000000000000

- **1.04**
  PCI BUS SINGLE DATA PHASE DISCONNECT CYCLES

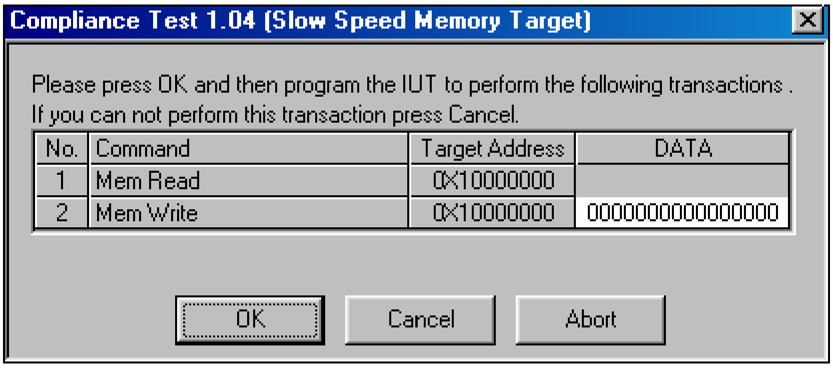
  The transactions of this section are similar to the section 1.02. The software will test for master disconnects.



Compliance Test 1.04 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

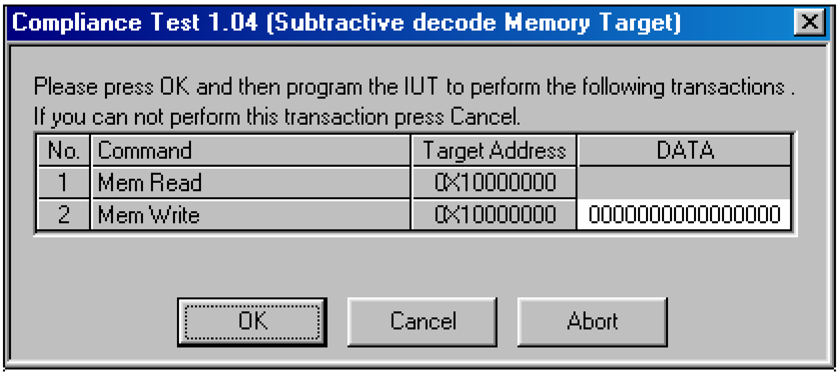
No.	Command	Target Address	DATA
1	Mem Read	0X10000000	
2	Mem Write	0X10000000	0000000000000000



Compliance Test 1.04 (Slow Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

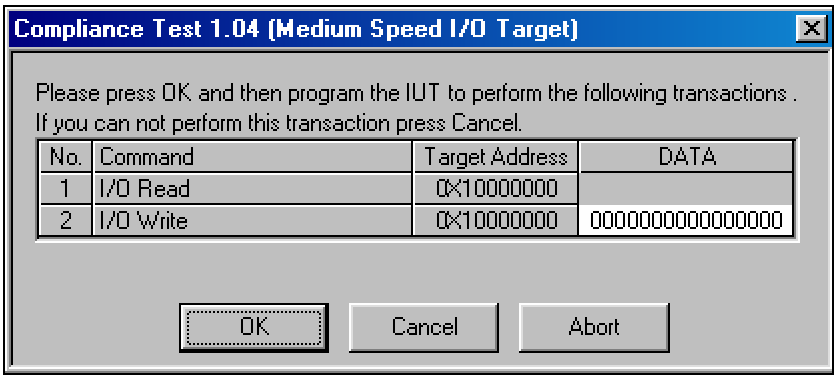
No.	Command	Target Address	DATA
1	Mem Read	0X10000000	
2	Mem Write	0X10000000	0000000000000000



Compliance Test 1.04 (Subtractive decode Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

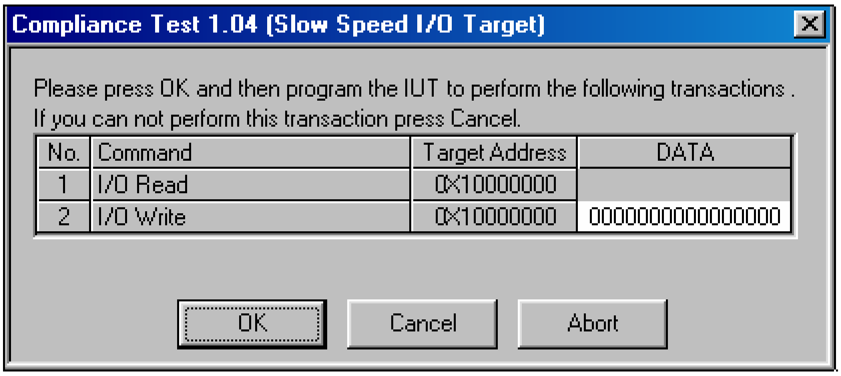
No.	Command	Target Address	DATA
1	Mem Read	0X10000000	
2	Mem Write	0X10000000	0000000000000000



Compliance Test 1.04 (Medium Speed I/O Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

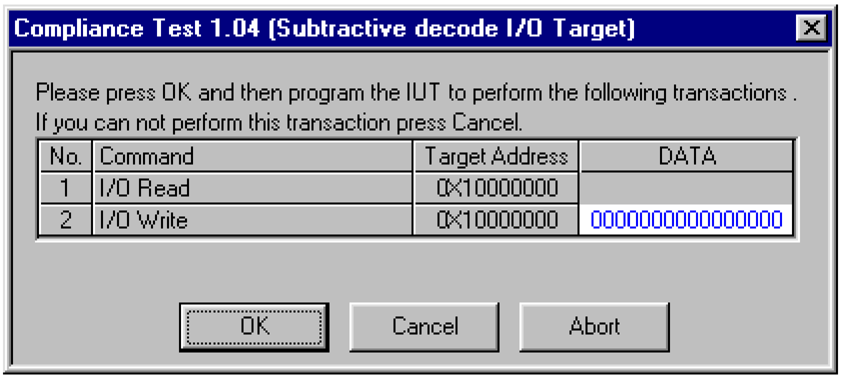
No.	Command	Target Address	DATA
1	I/O Read	0X10000000	
2	I/O Write	0X10000000	0000000000000000



Compliance Test 1.04 (Slow Speed I/O Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

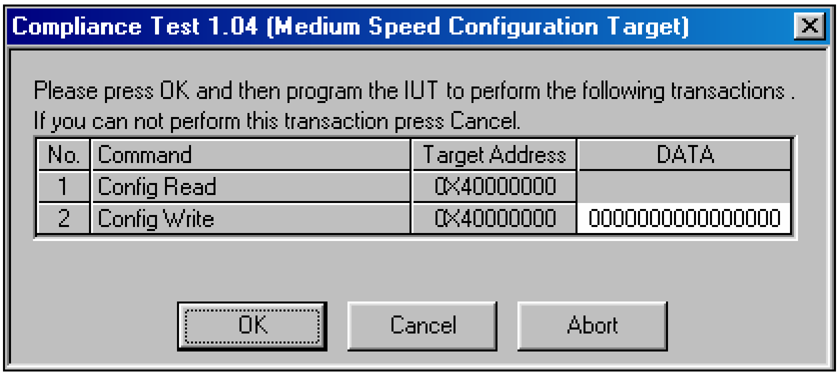
No.	Command	Target Address	DATA
1	I/O Read	0X10000000	
2	I/O Write	0X10000000	0000000000000000



Compliance Test 1.04 (Subtractive decode I/O Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

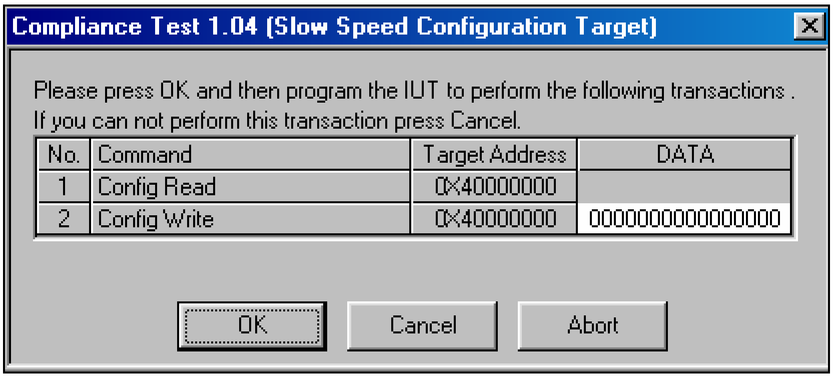
No.	Command	Target Address	DATA
1	I/O Read	0X10000000	
2	I/O Write	0X10000000	0000000000000000



Compliance Test 1.04 (Medium Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

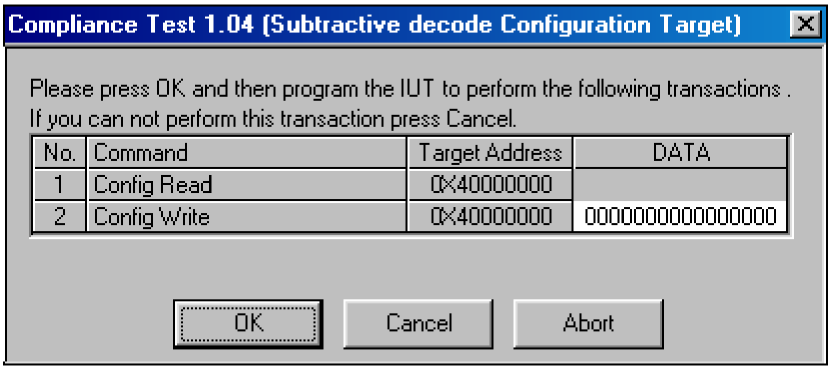
No.	Command	Target Address	DATA
1	Config Read	0X40000000	
2	Config Write	0X40000000	0000000000000000



Compliance Test 1.04 (Slow Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Config Read	0X40000000	
2	Config Write	0X40000000	0000000000000000



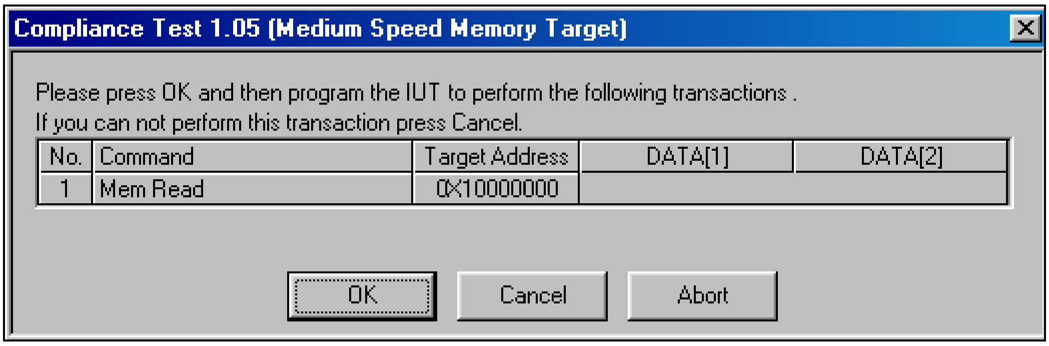
Compliance Test 1.04 (Subtractive decode Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Config Read	0X40000000	
2	Config Write	0X40000000	0000000000000000

- **1.05**
  PCI BUS MULTI-DATA PHASE TARGET ABORT CYCLES

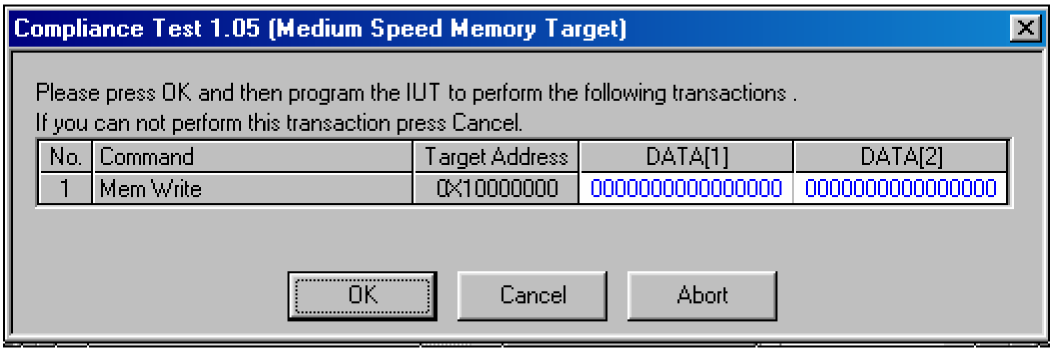
  There are five sets of transactions that must be executed in this test. The first set is a memory read command followed by a memory write command both with two data phases and the data of write command is 00000000H. This set is repeated three times. The second set is a configuration read followed by a configuration write command both with two data phases and the data of write command is 00000000H. This set is repeated three times. The third section is a memory read multiple command with three data phases that is repeated three times. The fourth section is a memory read line command with three data phases that is repeated three times. The last section is a memory write & invalidate command with three data phases (data value equal to 00000000H) that is repeated three times.



Compliance Test 1.05 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

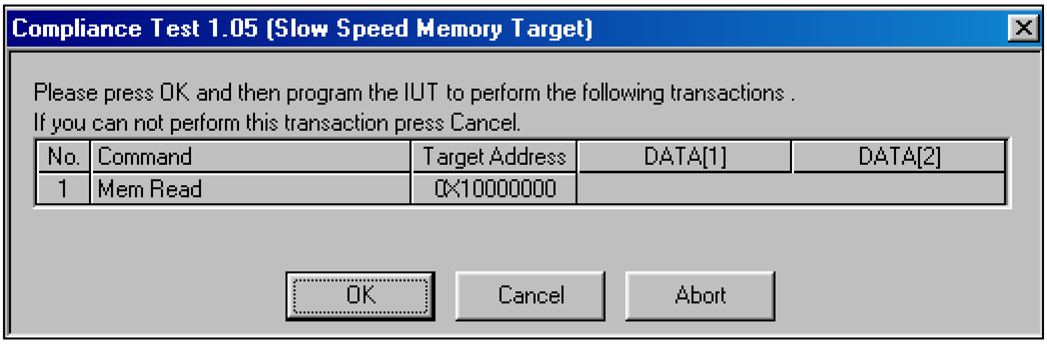
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read	0X10000000		



Compliance Test 1.05 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

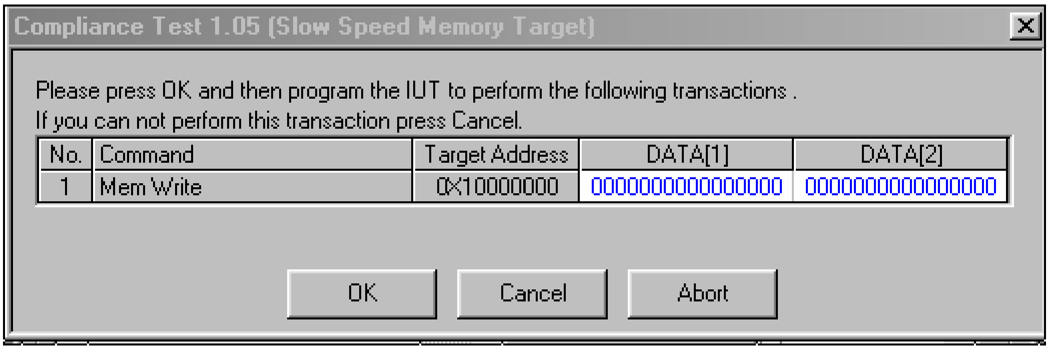
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write	0X10000000	0000000000000000	0000000000000000



Compliance Test 1.05 (Slow Speed Memory Target)

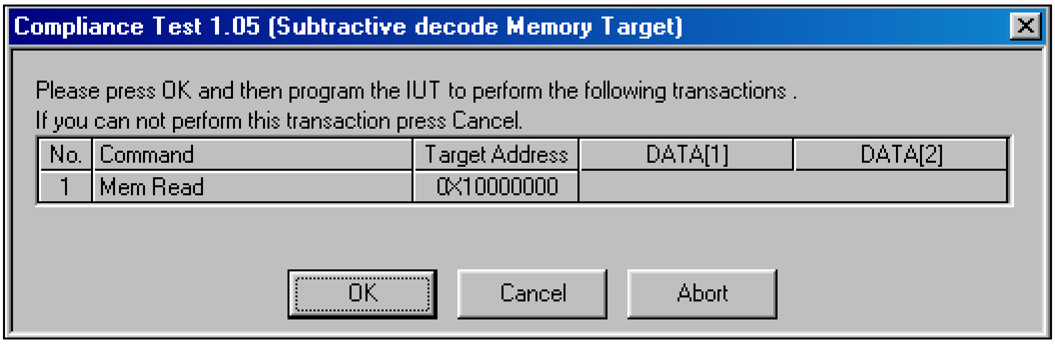
Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read	0X10000000		


Compliance Test 1.05 (Slow Speed Memory Target)

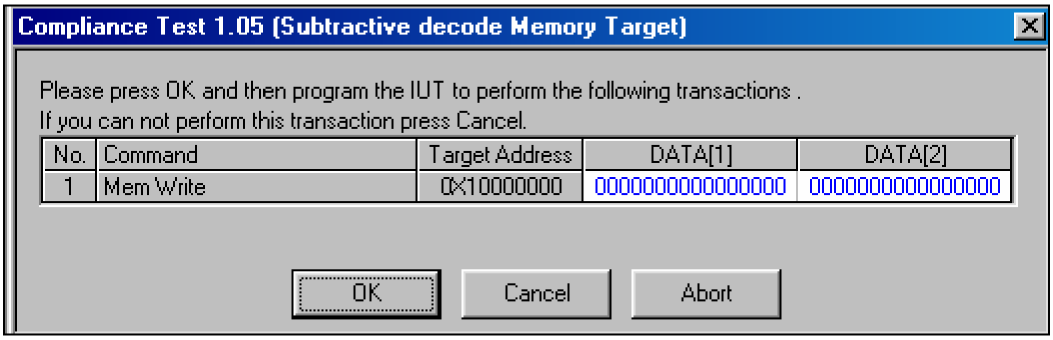
Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write	0X10000000	0000000000000000	0000000000000000


Compliance Test 1.05 (Subtractive decode Memory Target)

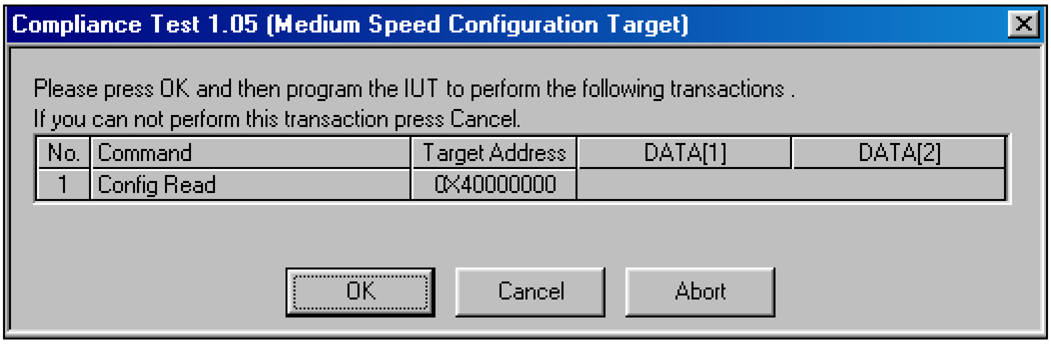
Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read	0X10000000		


Compliance Test 1.05 (Subtractive decode Memory Target)

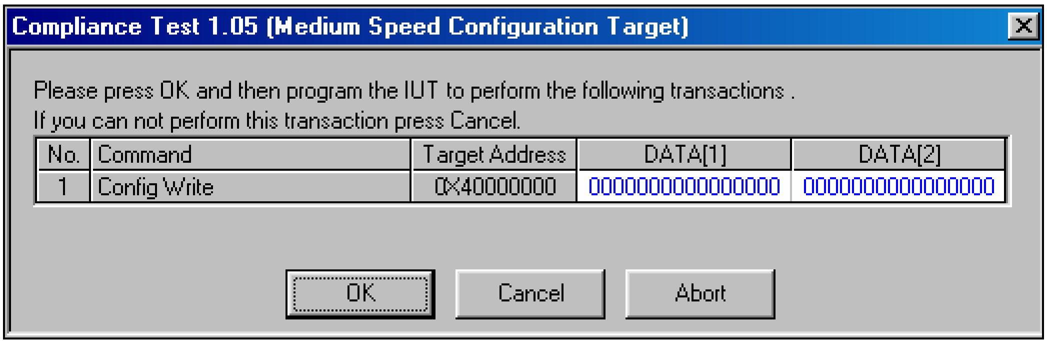
Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write	0X10000000	0000000000000000	0000000000000000


Compliance Test 1.05 (Medium Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

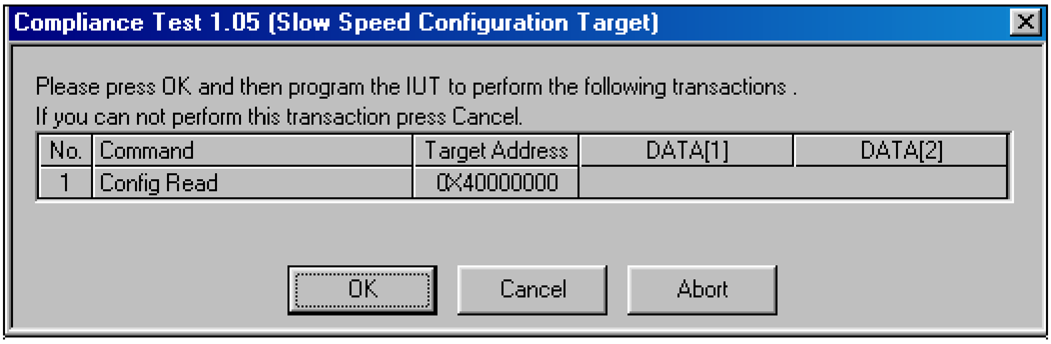
No.	Command	Target Address	DATA[1]	DATA[2]
1	Config Read	0X40000000		



Compliance Test 1.05 (Medium Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

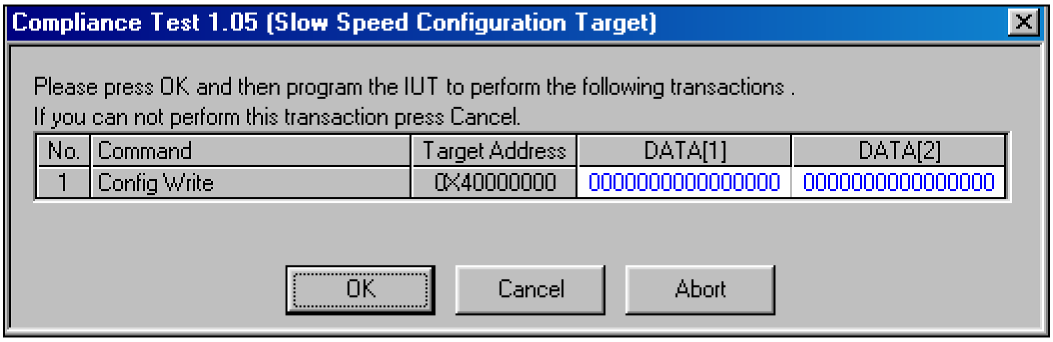
No.	Command	Target Address	DATA[1]	DATA[2]
1	Config Write	0X40000000	0000000000000000	0000000000000000



Compliance Test 1.05 (Slow Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

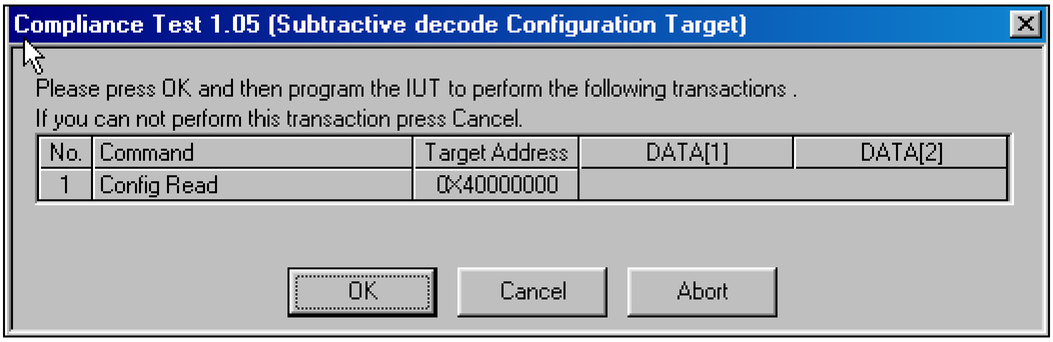
No.	Command	Target Address	DATA[1]	DATA[2]
1	Config Read	0X40000000		



Compliance Test 1.05 (Slow Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

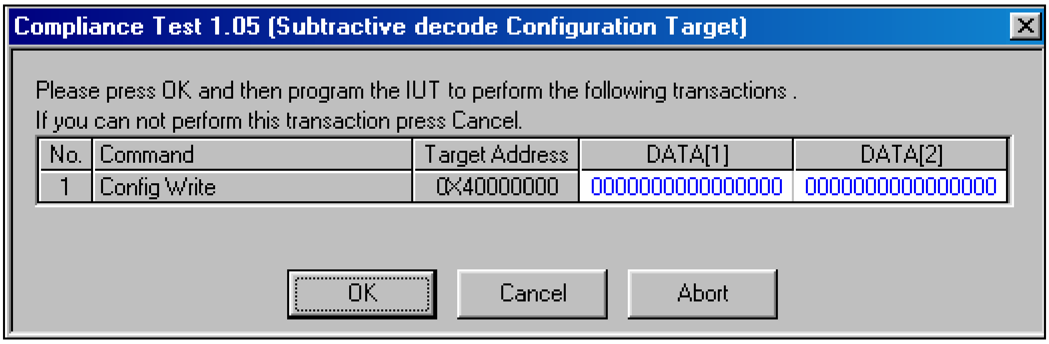
No.	Command	Target Address	DATA[1]	DATA[2]
1	Config Write	0X40000000	0000000000000000	0000000000000000



Compliance Test 1.05 (Subtractive decode Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

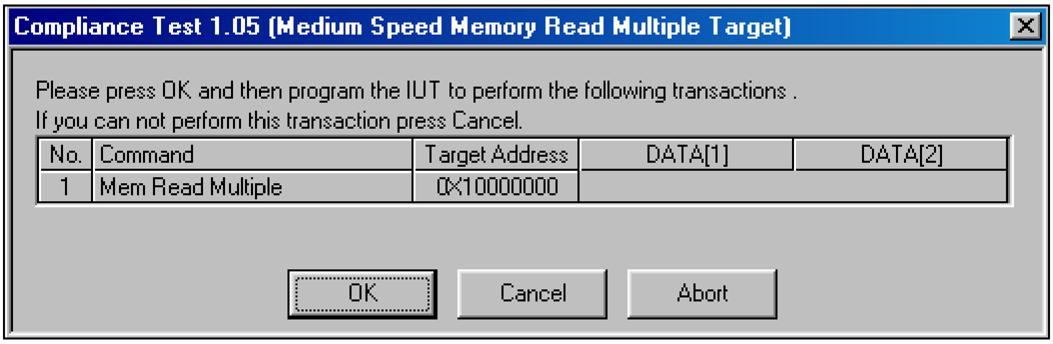
No.	Command	Target Address	DATA[1]	DATA[2]
1	Config Read	0X40000000		



Compliance Test 1.05 (Subtractive decode Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

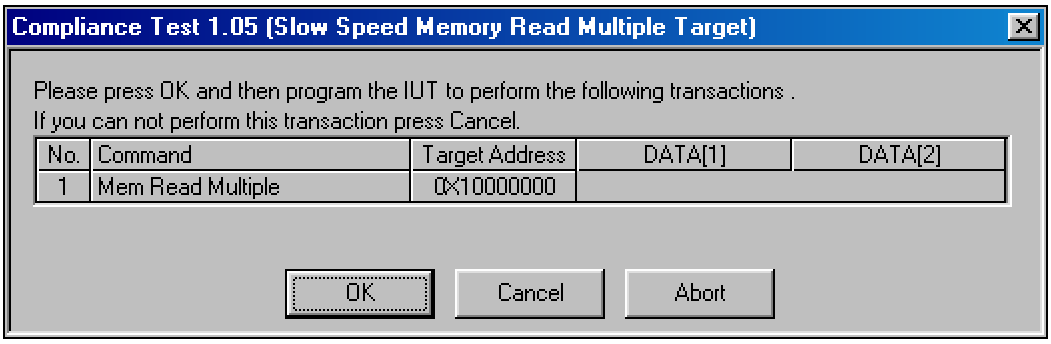
No.	Command	Target Address	DATA[1]	DATA[2]
1	Config Write	0X40000000	0000000000000000	0000000000000000



Compliance Test 1.05 (Medium Speed Memory Read Multiple Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

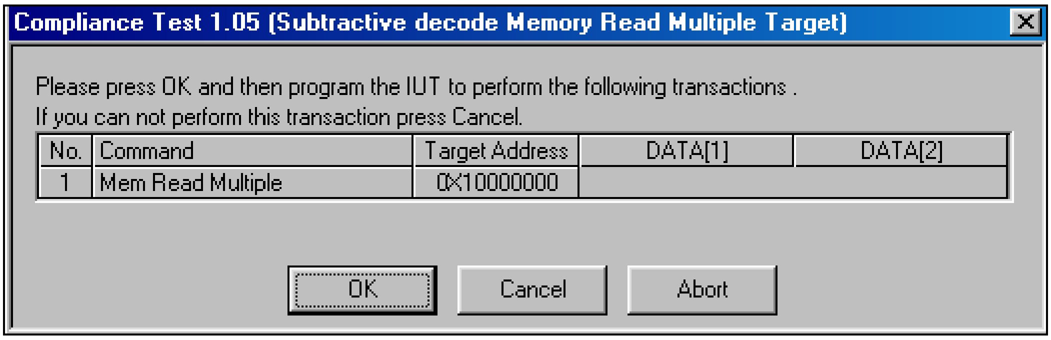
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Multiple	0X10000000		



Compliance Test 1.05 (Slow Speed Memory Read Multiple Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

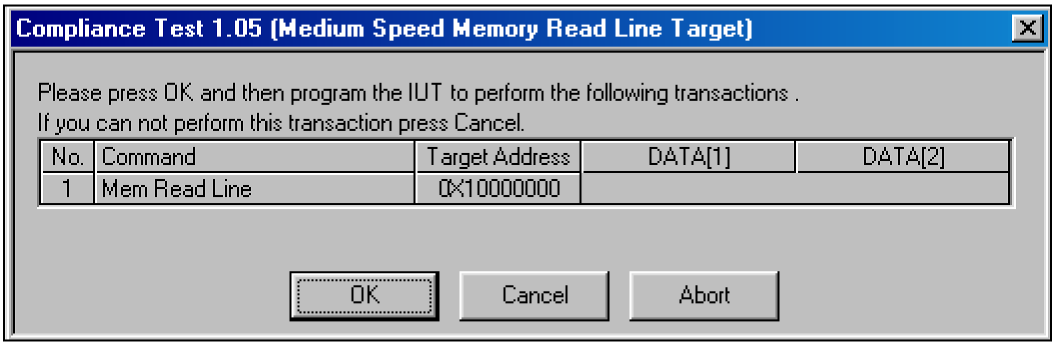
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Multiple	0X10000000		



Compliance Test 1.05 (Subtractive decode Memory Read Multiple Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

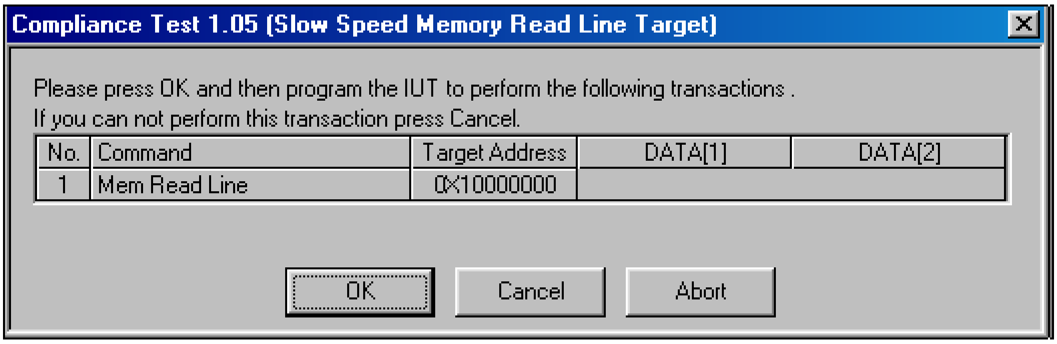
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Multiple	0X10000000		



Compliance Test 1.05 (Medium Speed Memory Read Line Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

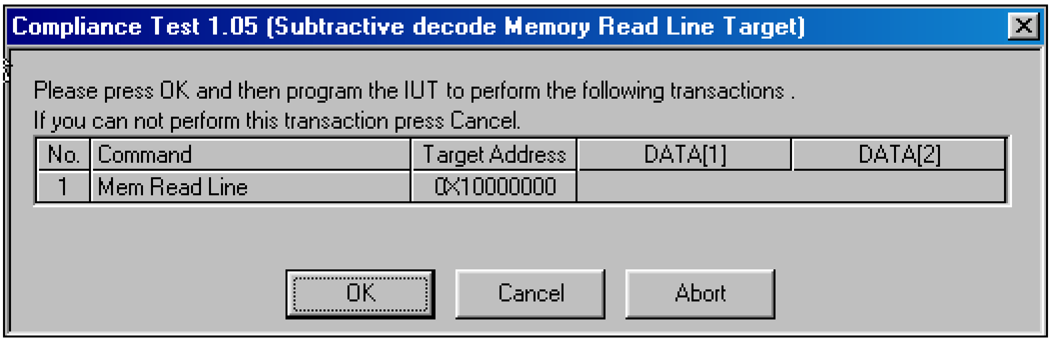
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Line	0X10000000		



Compliance Test 1.05 (Slow Speed Memory Read Line Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

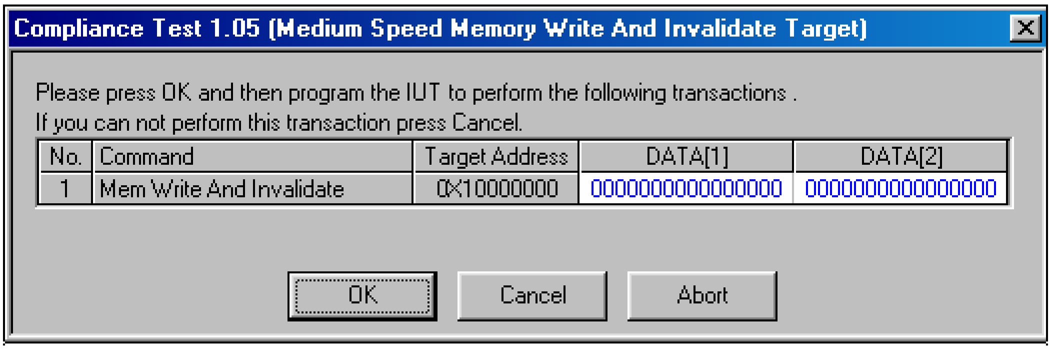
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Line	0X10000000		



Compliance Test 1.05 (Subtractive decode Memory Read Line Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

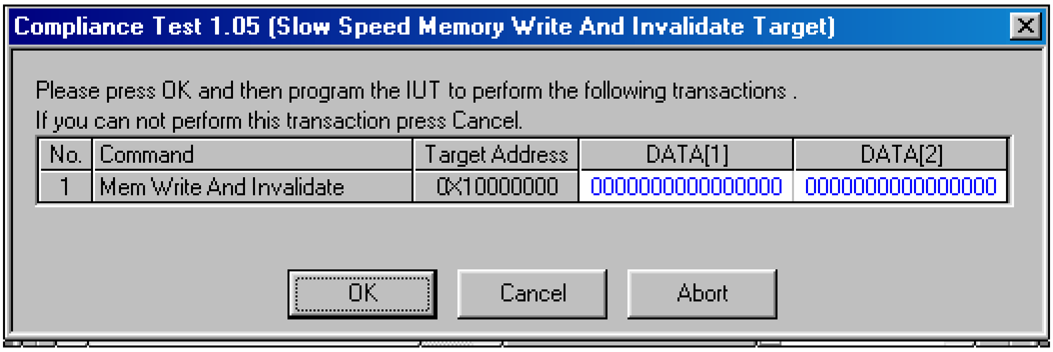
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Line	0X10000000		



Compliance Test 1.05 (Medium Speed Memory Write And Invalidate Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

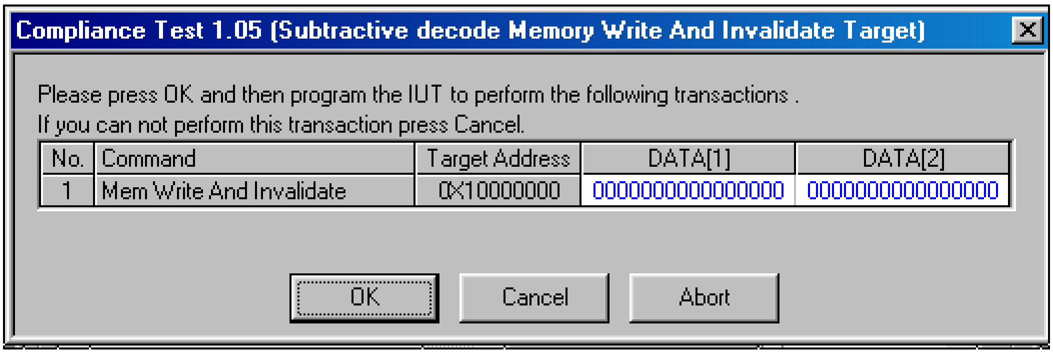
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write And Invalidate	0X10000000	0000000000000000	0000000000000000



Compliance Test 1.05 (Slow Speed Memory Write And Invalidate Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write And Invalidate	0X10000000	0000000000000000	0000000000000000



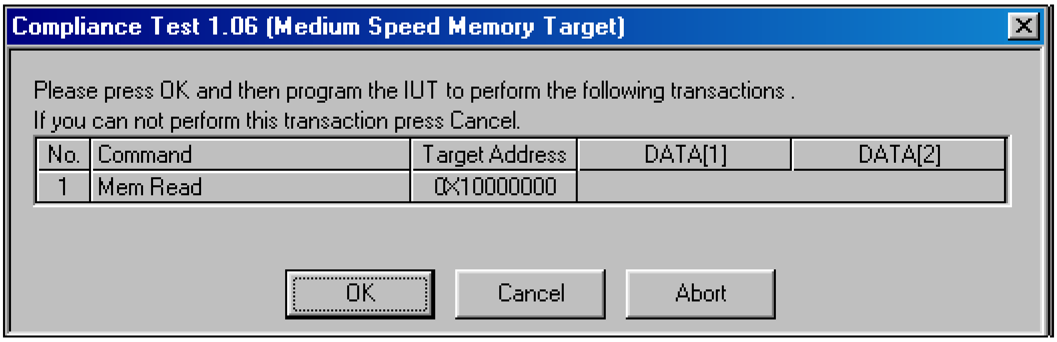
Compliance Test 1.05 (Subtractive decode Memory Write And Invalidate Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write And Invalidate	0X10000000	0000000000000000	0000000000000000

- **1.06**
  PCI BUS MULTI-DATA PHASE RETRY CYCLES

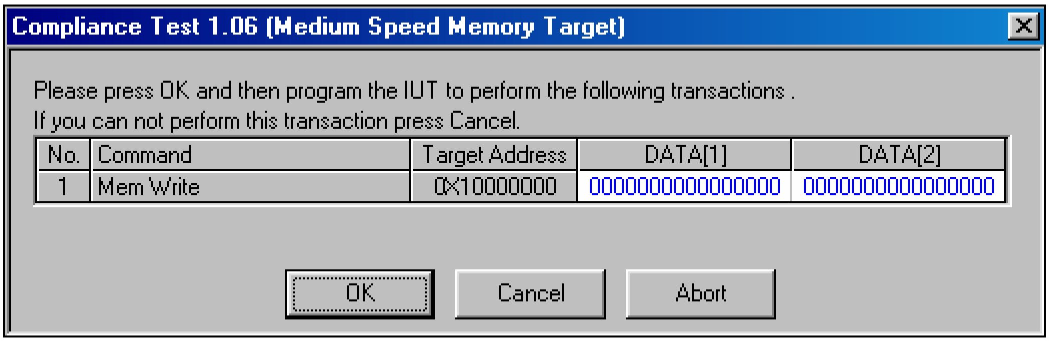
The transactions of this section are similar to the previous section (1.05) The software will test for master retry, some messages include confirmation from the user.



Compliance Test 1.06 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

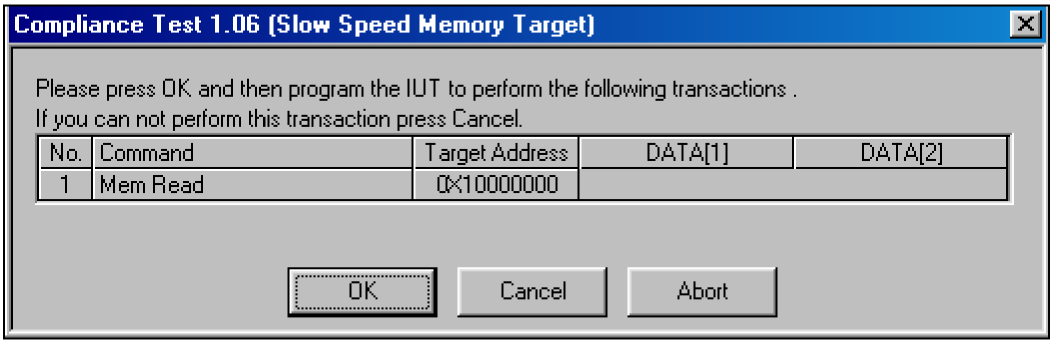
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read	0X10000000		



Compliance Test 1.06 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

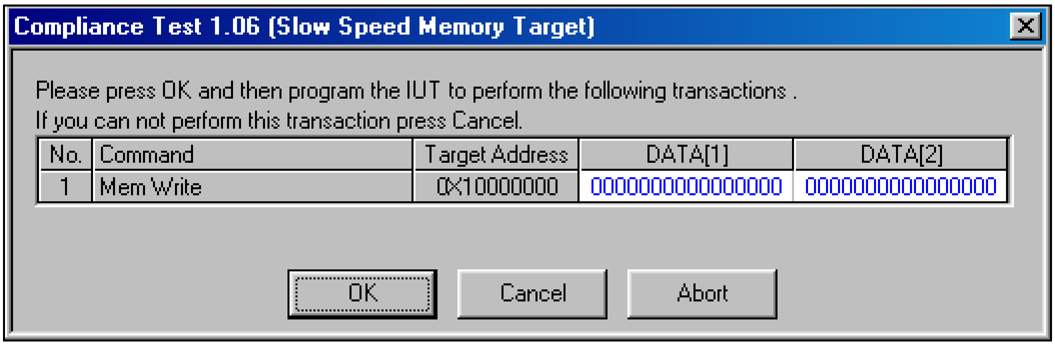
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write	0X10000000	0000000000000000	0000000000000000



Compliance Test 1.06 (Slow Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

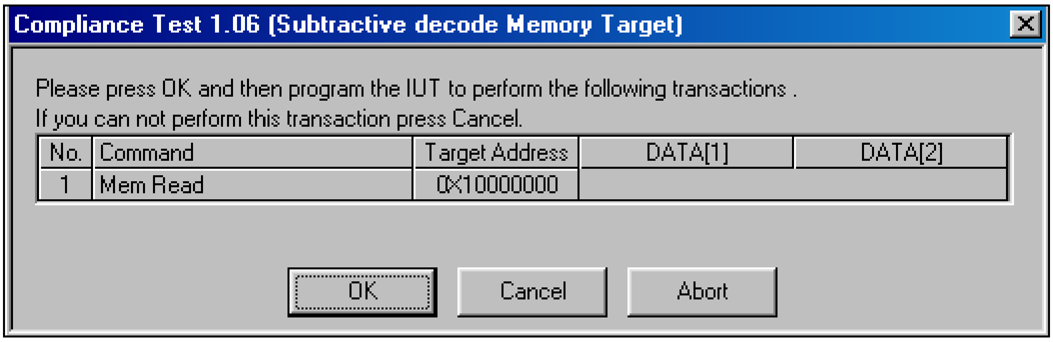
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read	0X10000000		



Compliance Test 1.06 (Slow Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

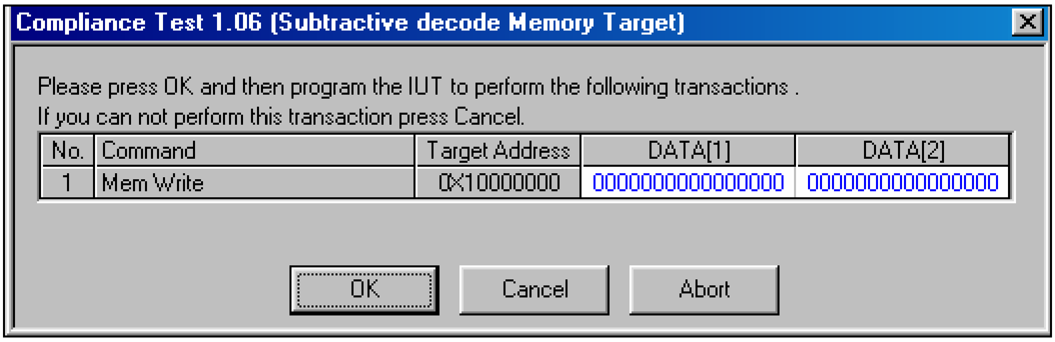
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write	0X10000000	0000000000000000	0000000000000000



Compliance Test 1.06 (Subtractive decode Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

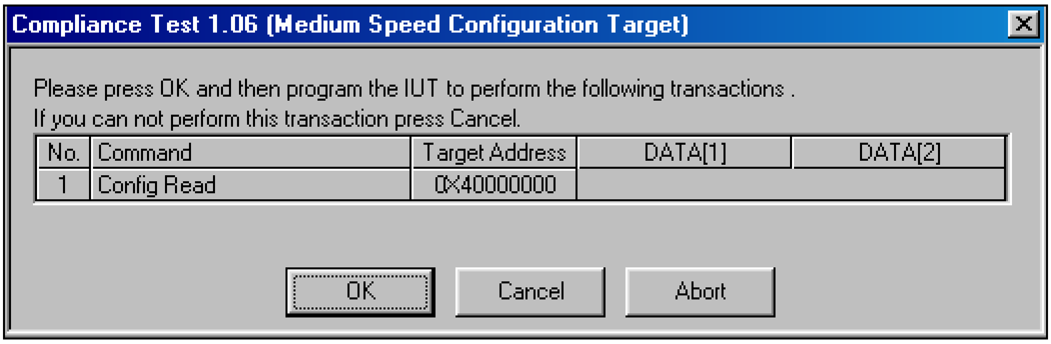
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read	0X10000000		



Compliance Test 1.06 (Subtractive decode Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

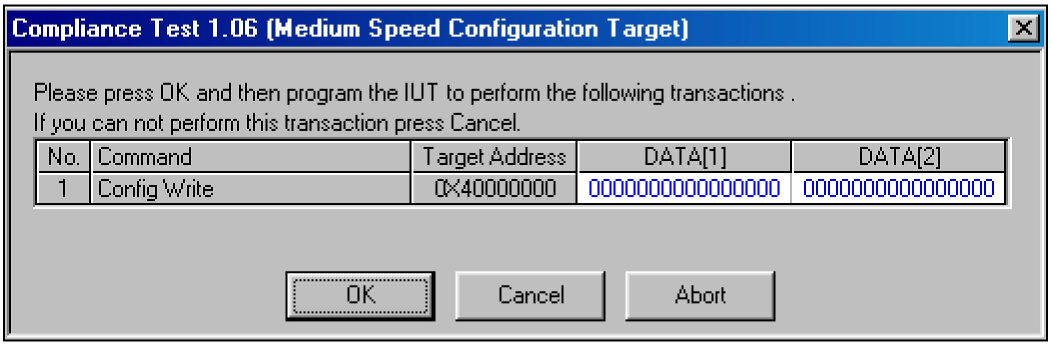
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write	0X10000000	0000000000000000	0000000000000000



Compliance Test 1.06 (Medium Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

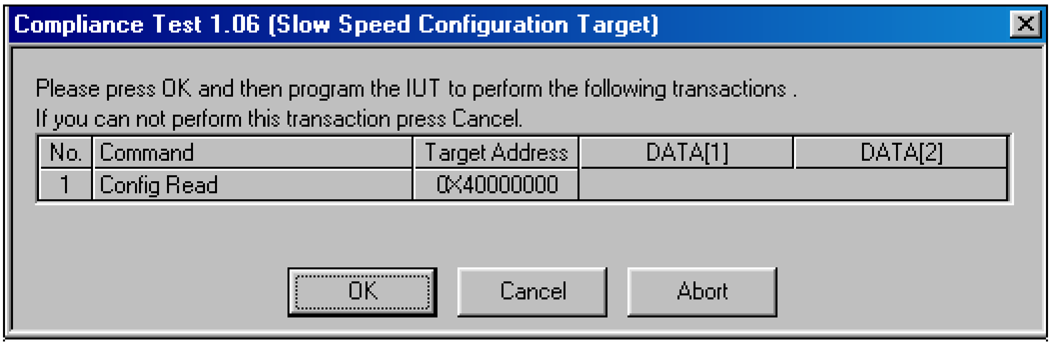
No.	Command	Target Address	DATA[1]	DATA[2]
1	Config Read	0X40000000		



Compliance Test 1.06 (Medium Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

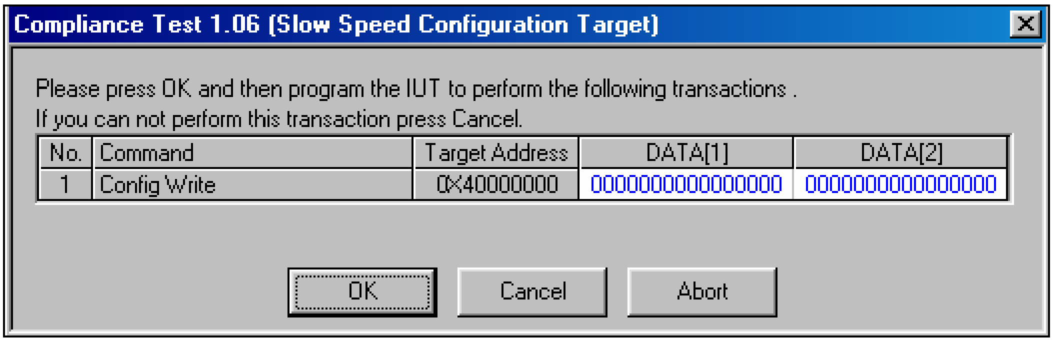
No.	Command	Target Address	DATA[1]	DATA[2]
1	Config Write	0X40000000	0000000000000000	0000000000000000



Compliance Test 1.06 (Slow Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

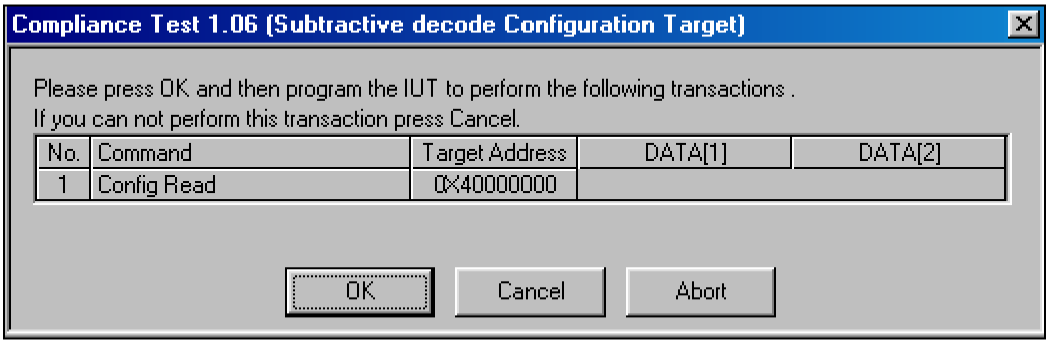
No.	Command	Target Address	DATA[1]	DATA[2]
1	Config Read	0X40000000		



Compliance Test 1.06 (Slow Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

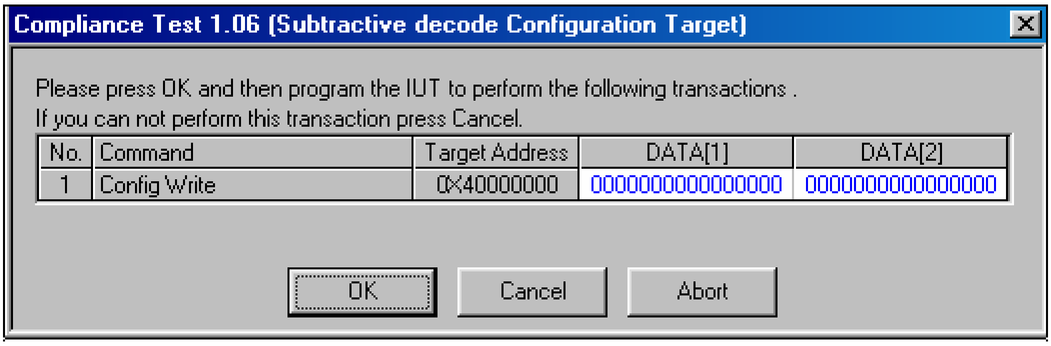
No.	Command	Target Address	DATA[1]	DATA[2]
1	Config Write	0X40000000	0000000000000000	0000000000000000



Compliance Test 1.06 (Subtractive decode Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

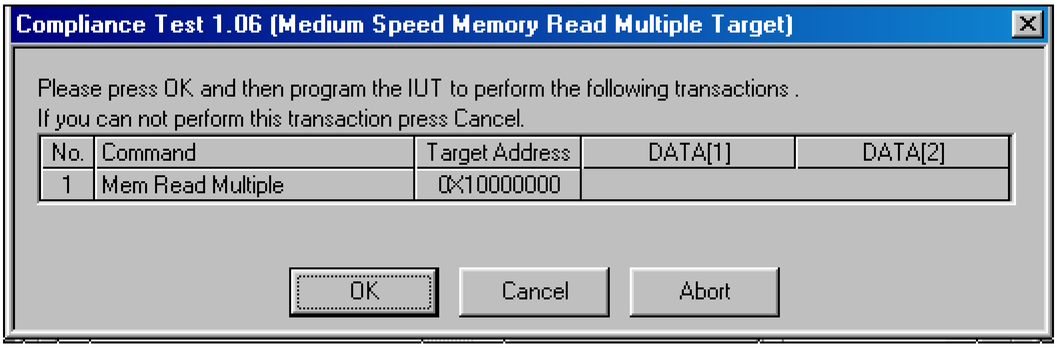
No.	Command	Target Address	DATA[1]	DATA[2]
1	Config Read	0X40000000		



Compliance Test 1.06 (Subtractive decode Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

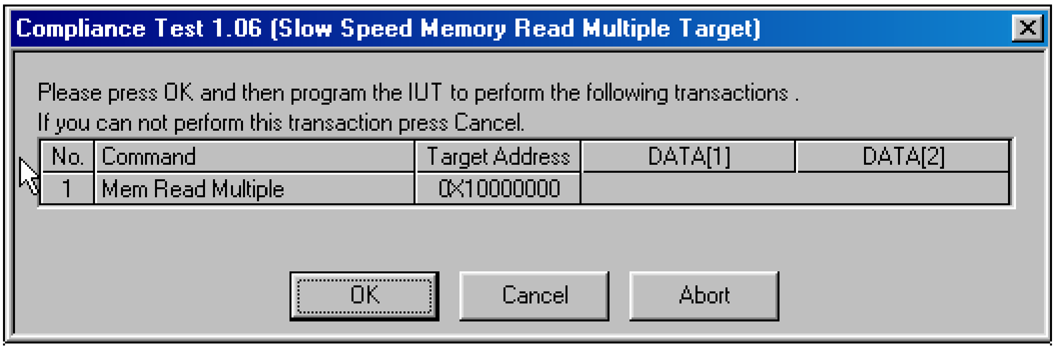
No.	Command	Target Address	DATA[1]	DATA[2]
1	Config Write	0X40000000	0000000000000000	0000000000000000



Compliance Test 1.06 (Medium Speed Memory Read Multiple Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

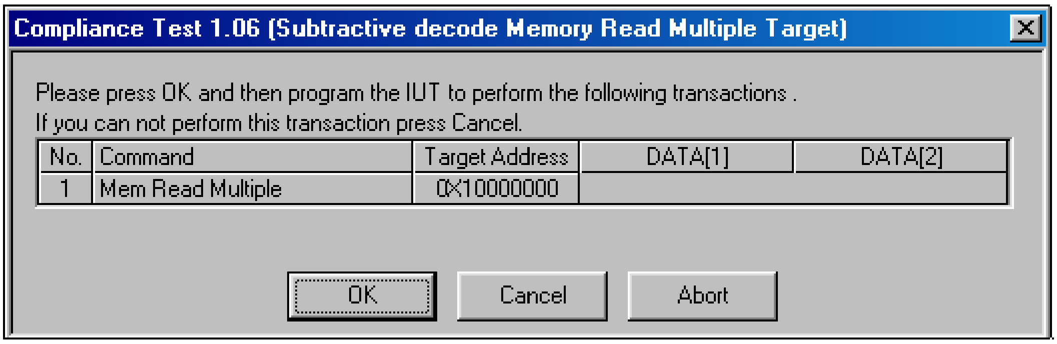
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Multiple	0X10000000		



Compliance Test 1.06 (Slow Speed Memory Read Multiple Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

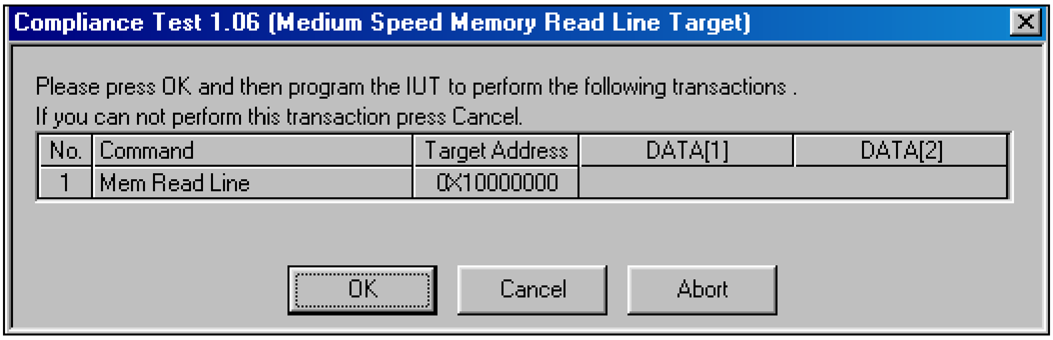
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Multiple	0X10000000		



Compliance Test 1.06 (Subtractive decode Memory Read Multiple Target)

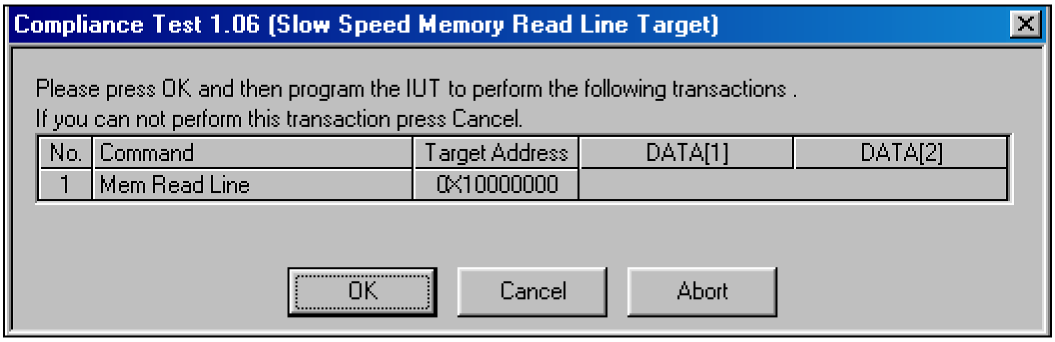
Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Multiple	0X10000000		


Compliance Test 1.06 (Medium Speed Memory Read Line Target)

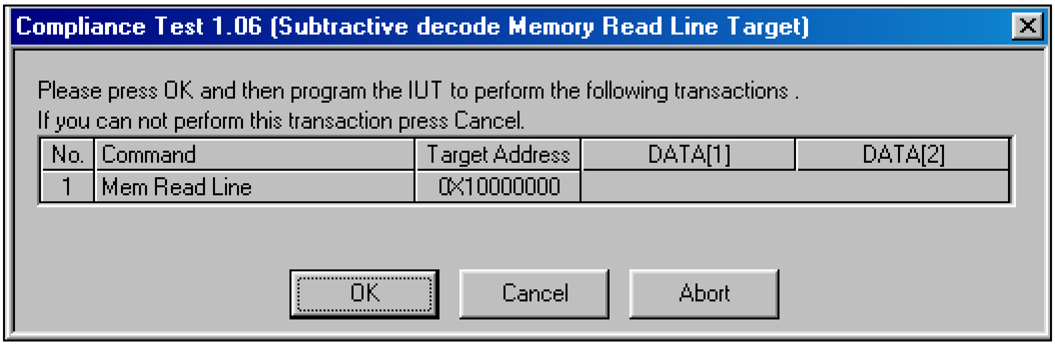
Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Line	0X10000000		


Compliance Test 1.06 (Slow Speed Memory Read Line Target)

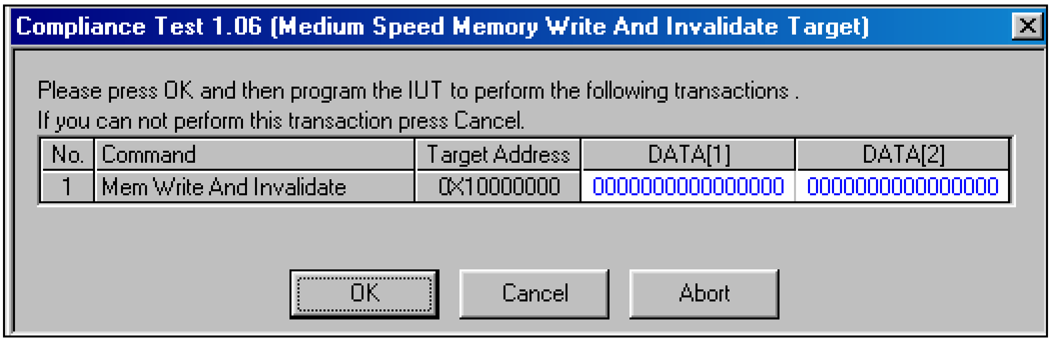
Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Line	0X10000000		


Compliance Test 1.06 (Subtractive decode Memory Read Line Target)

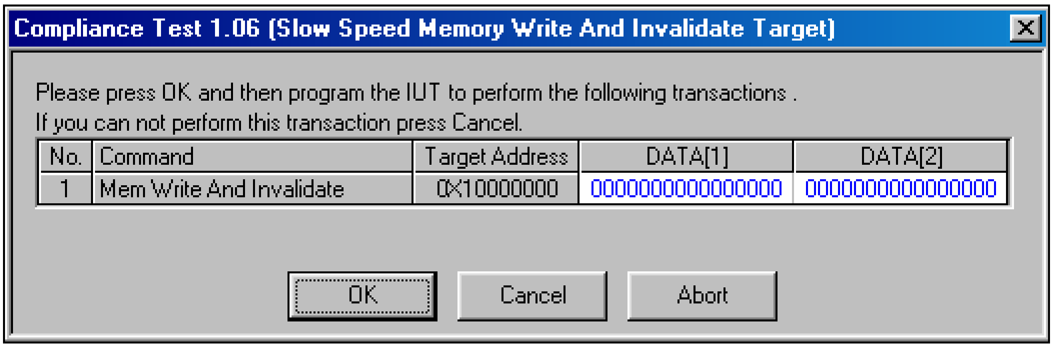
Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Line	0X10000000		


Compliance Test 1.06 (Medium Speed Memory Write And Invalidate Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

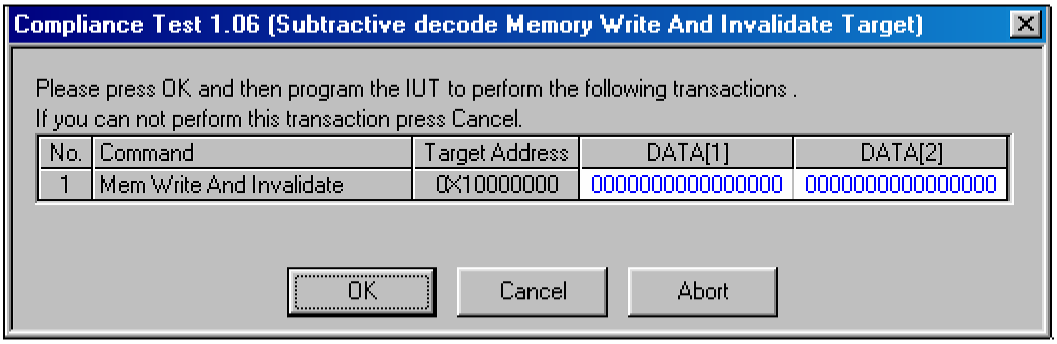
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write And Invalidate	0X10000000	0000000000000000	0000000000000000



Compliance Test 1.06 (Slow Speed Memory Write And Invalidate Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write And Invalidate	0X10000000	0000000000000000	0000000000000000



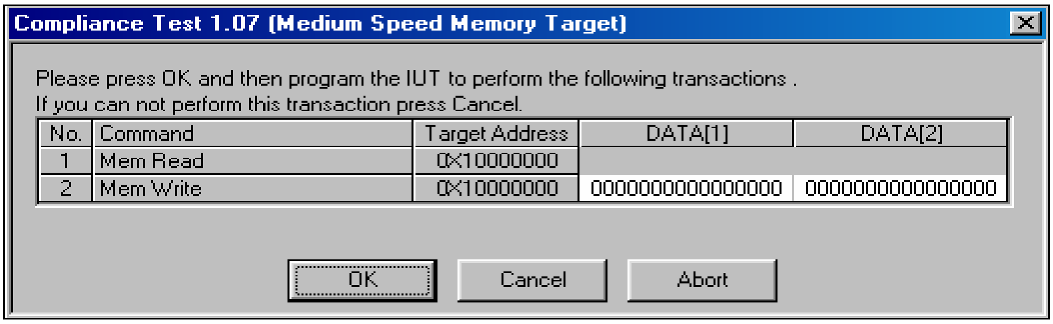
Compliance Test 1.06 (Subtractive decode Memory Write And Invalidate Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write And Invalidate	0X10000000	0000000000000000	0000000000000000

- **1.07**
  PCI BUS MULTI-DATA PHASE DISCONNECT CYCLES

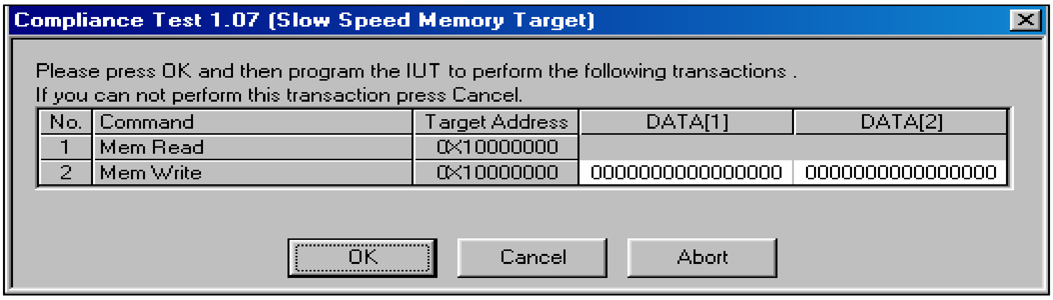
  The transactions of this section are similar to the previous section (1.06). The software will test for master disconnects.



Compliance Test 1.07 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

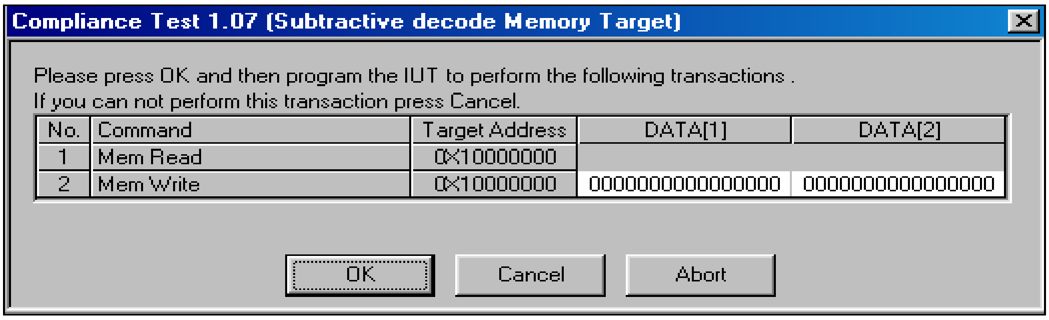
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read	0X10000000		
2	Mem Write	0X10000000	0000000000000000	0000000000000000



Compliance Test 1.07 (Slow Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

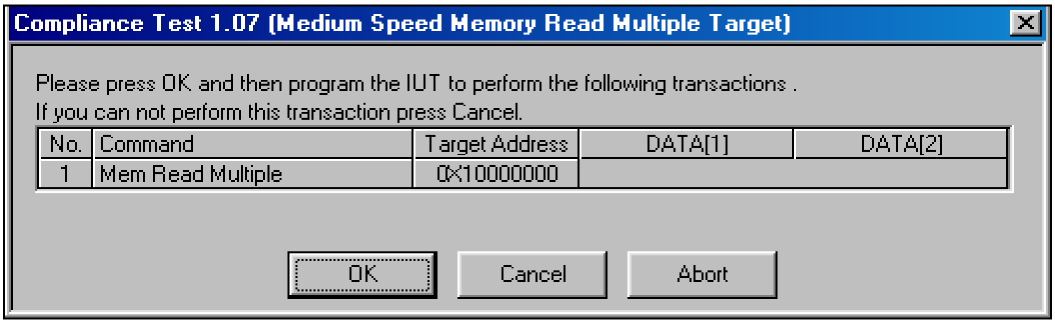
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read	0X10000000		
2	Mem Write	0X10000000	0000000000000000	0000000000000000



Compliance Test 1.07 (Subtractive decode Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

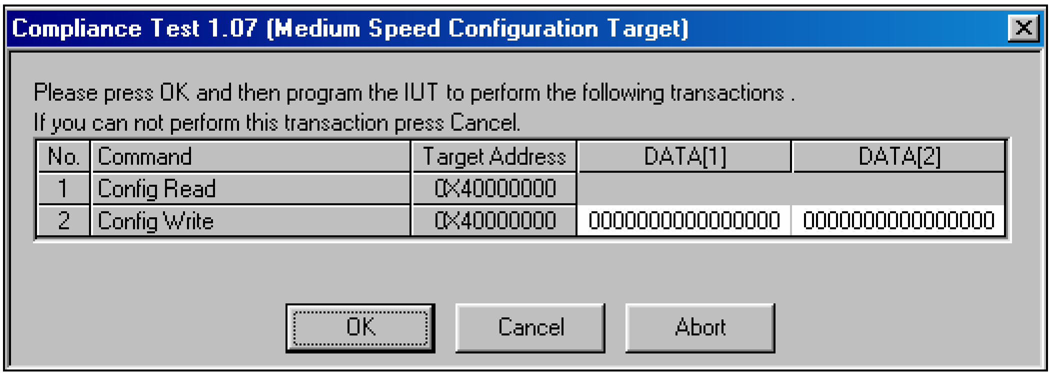
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read	0X10000000		
2	Mem Write	0X10000000	0000000000000000	0000000000000000



Compliance Test 1.07 (Medium Speed Memory Read Multiple Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

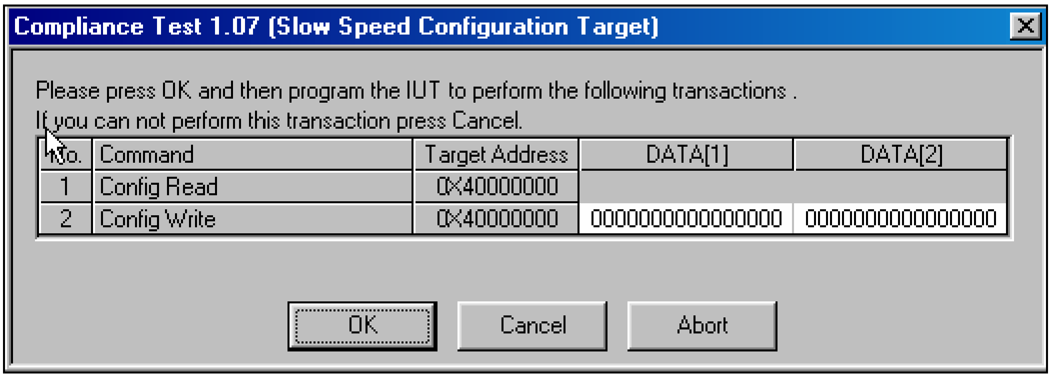
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Multiple	0X10000000		



Compliance Test 1.07 (Medium Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

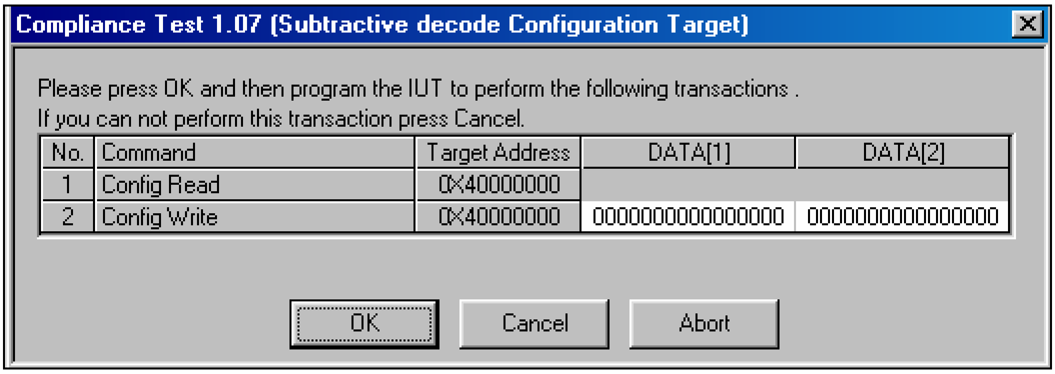
No.	Command	Target Address	DATA[1]	DATA[2]
1	Config Read	0X40000000		
2	Config Write	0X40000000	0000000000000000	0000000000000000



Compliance Test 1.07 (Slow Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

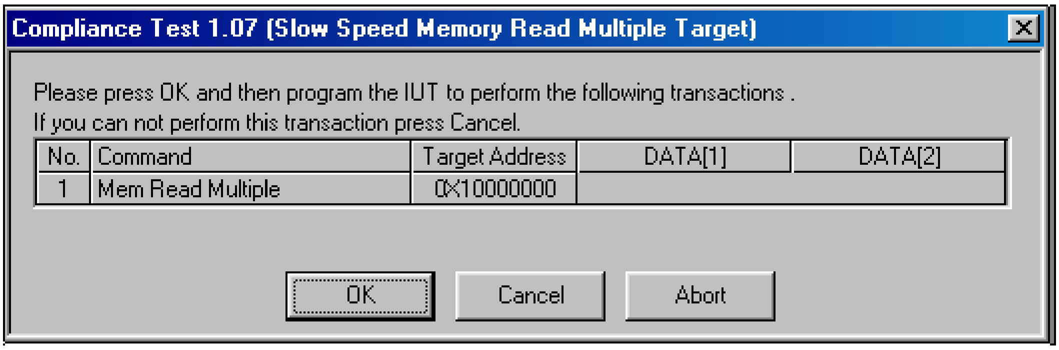
No.	Command	Target Address	DATA[1]	DATA[2]
1	Config Read	0X40000000		
2	Config Write	0X40000000	0000000000000000	0000000000000000



Compliance Test 1.07 (Subtractive decode Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

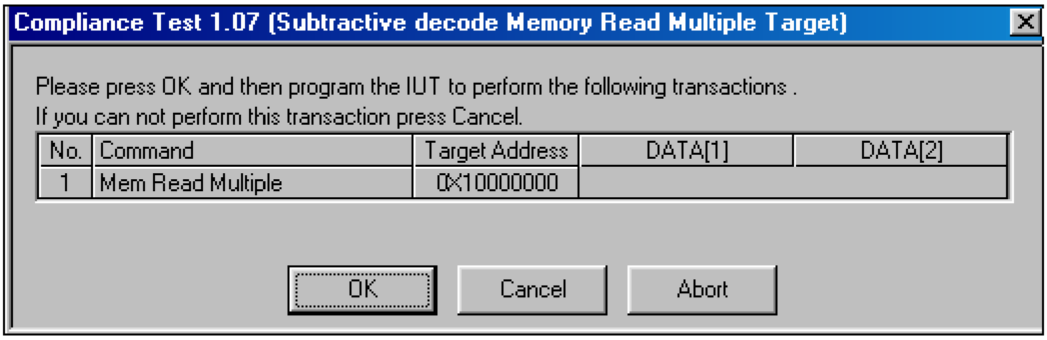
No.	Command	Target Address	DATA[1]	DATA[2]
1	Config Read	0X40000000		
2	Config Write	0X40000000	0000000000000000	0000000000000000



Compliance Test 1.07 (Slow Speed Memory Read Multiple Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

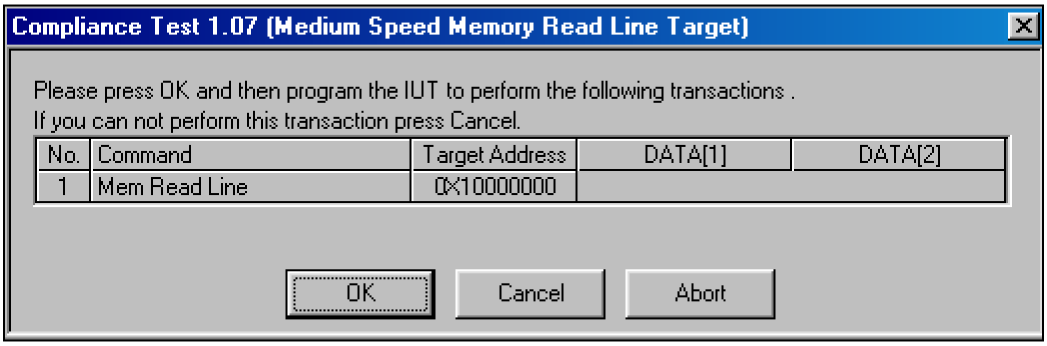
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Multiple	0X10000000		



Compliance Test 1.07 (Subtractive decode Memory Read Multiple Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

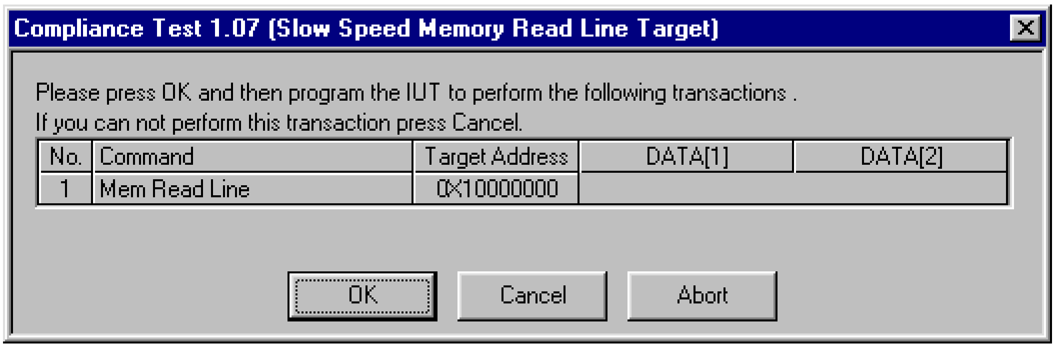
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Multiple	0X10000000		



Compliance Test 1.07 (Medium Speed Memory Read Line Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

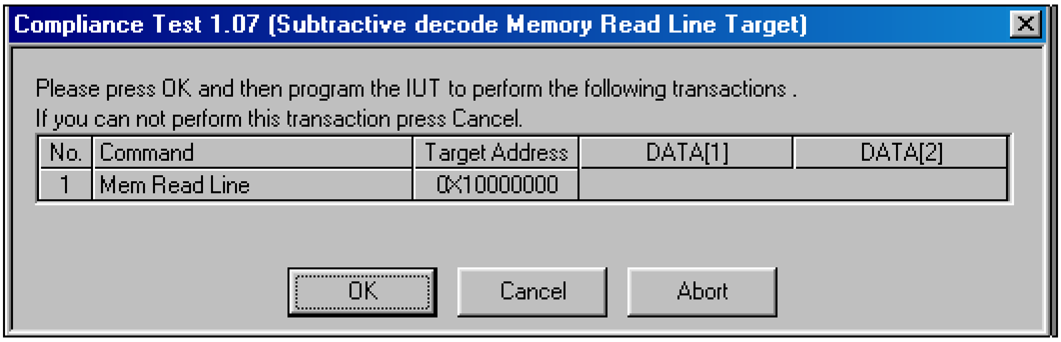
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Line	0X10000000		



Compliance Test 1.07 (Slow Speed Memory Read Line Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

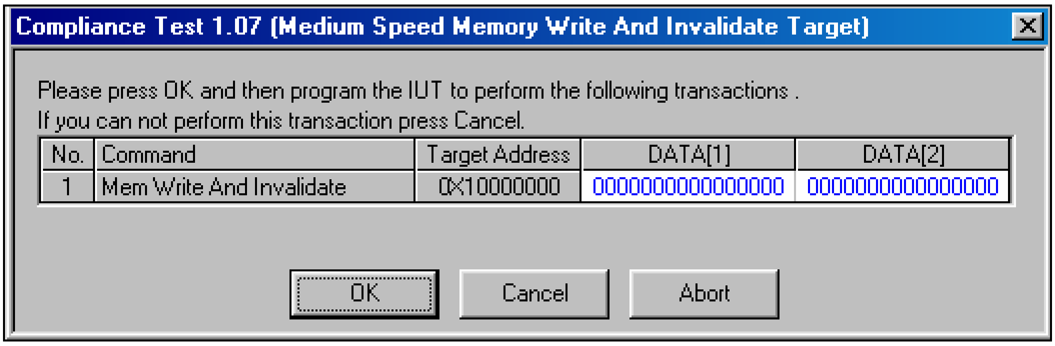
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Line	0X10000000		



Compliance Test 1.07 (Subtractive decode Memory Read Line Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

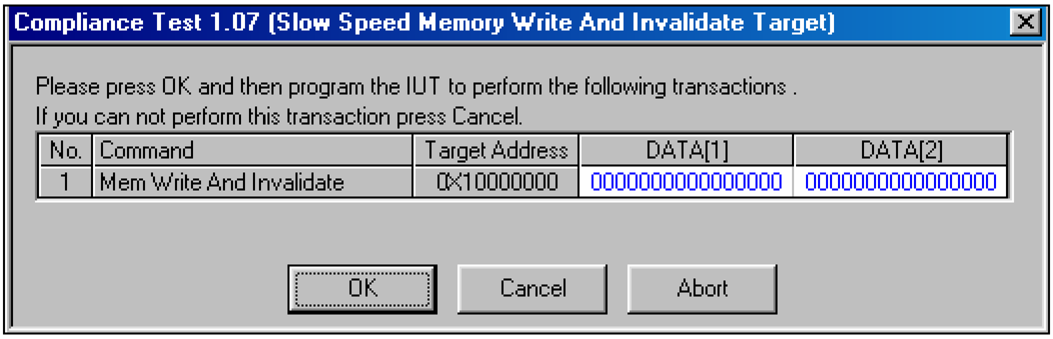
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Line	0X10000000		



Compliance Test 1.07 (Medium Speed Memory Write And Invalidate Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

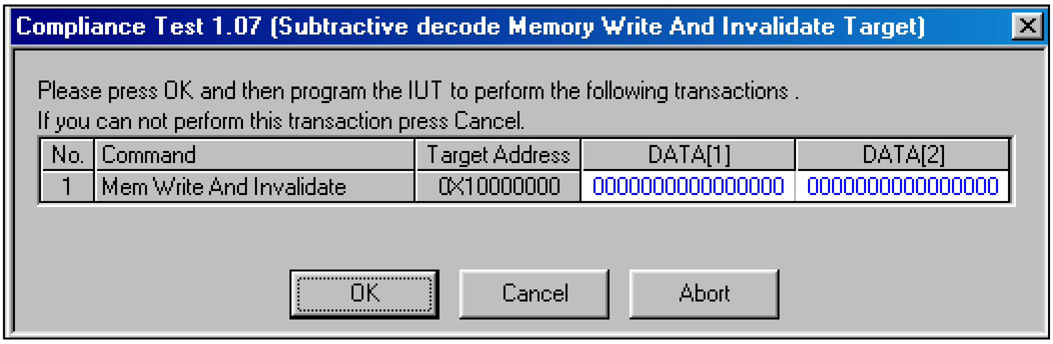
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write And Invalidate	0X10000000	0000000000000000	0000000000000000



Compliance Test 1.07 (Slow Speed Memory Write And Invalidate Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write And Invalidate	0X10000000	0000000000000000	0000000000000000



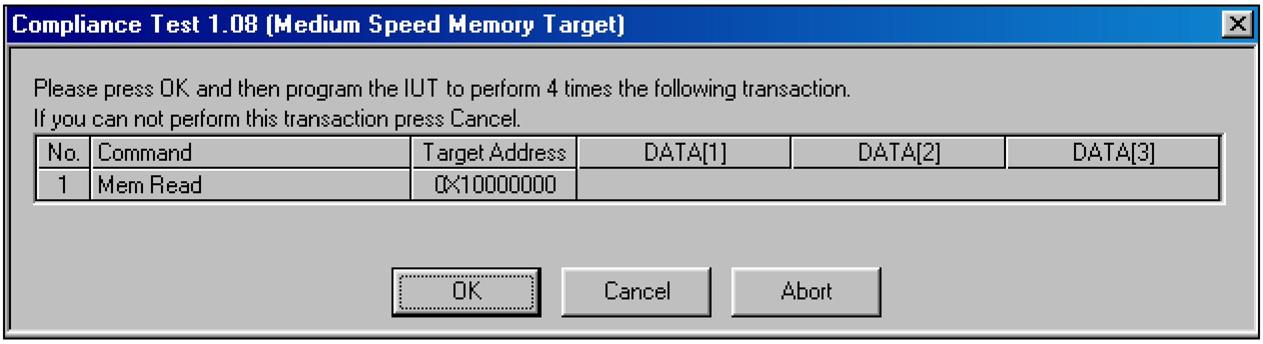
Compliance Test 1.07 (Subtractive decode Memory Write And Invalidate Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write And Invalidate	0X10000000	0000000000000000	0000000000000000

- **1.08**
  PCI BUS MULTI-DATA PHASE & TRDY# CYCLES

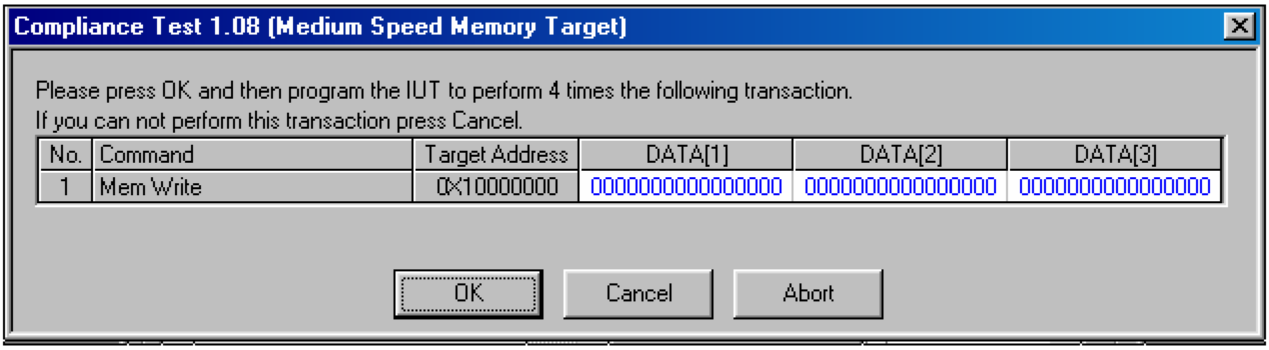
  In this test five transactions must be executed. The first is a memory read, the second is a memory write, the third is a memory read multiple, the fourth is a memory read line and the last is a memory write & invalidate. All transactions have three data phases.



Compliance Test 1.08 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform 4 times the following transaction.
If you can not perform this transaction press Cancel.

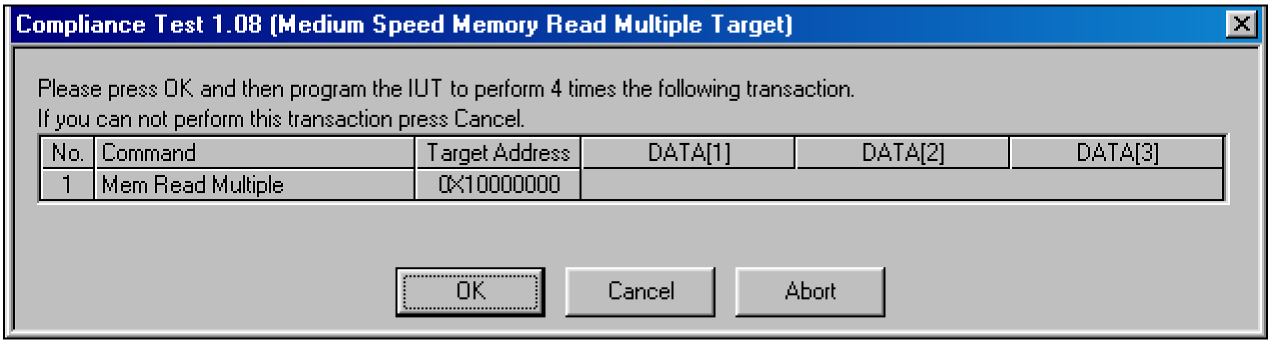
No.	Command	Target Address	DATA[1]	DATA[2]	DATA[3]
1	Mem Read	0X10000000			



Compliance Test 1.08 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform 4 times the following transaction.
If you can not perform this transaction press Cancel.

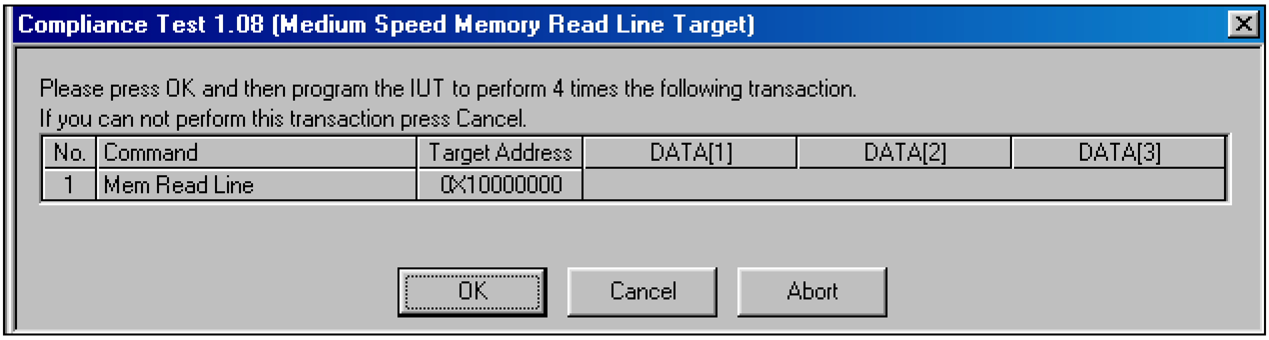
No.	Command	Target Address	DATA[1]	DATA[2]	DATA[3]
1	Mem Write	0X10000000	0000000000000000	0000000000000000	0000000000000000



Compliance Test 1.08 (Medium Speed Memory Read Multiple Target)

Please press OK and then program the IUT to perform 4 times the following transaction.
If you can not perform this transaction press Cancel.

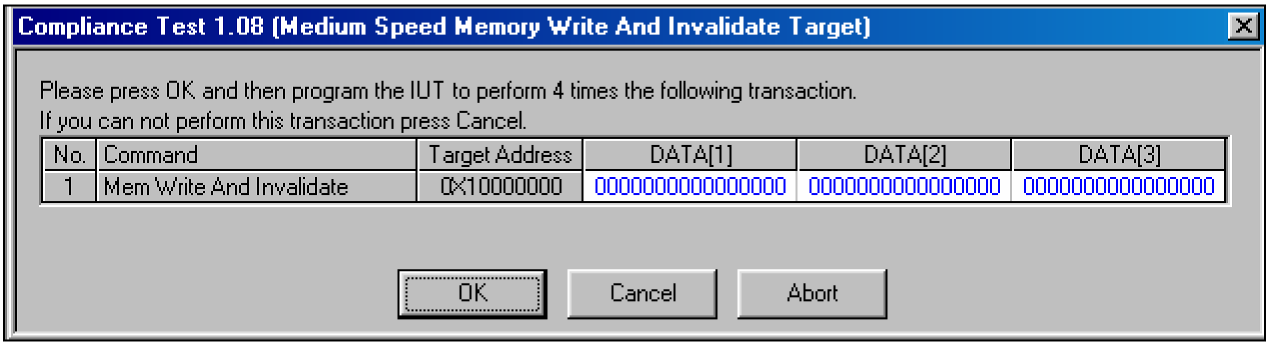
No.	Command	Target Address	DATA[1]	DATA[2]	DATA[3]
1	Mem Read Multiple	0X10000000			



Compliance Test 1.08 (Medium Speed Memory Read Line Target)

Please press OK and then program the IUT to perform 4 times the following transaction.
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]	DATA[3]
1	Mem Read Line	0X10000000			



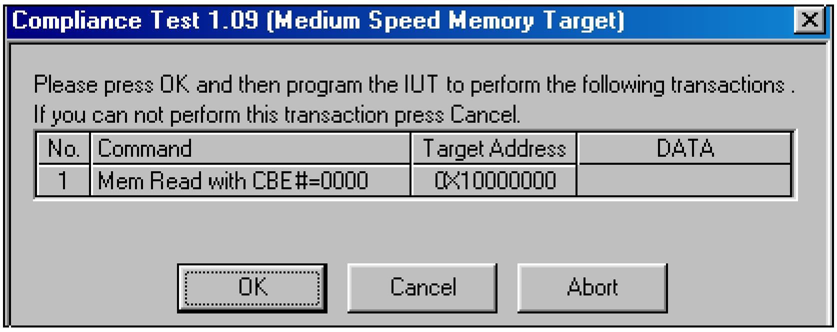
Compliance Test 1.08 (Medium Speed Memory Write And Invalidate Target)

Please press OK and then program the IUT to perform 4 times the following transaction.
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]	DATA[3]
1	Mem Write And Invalidate	0X10000000	0000000000000000	0000000000000000	0000000000000000

- **1.09**
  PCI BUS DATA PARITY ERROR SINGLE CYCLES

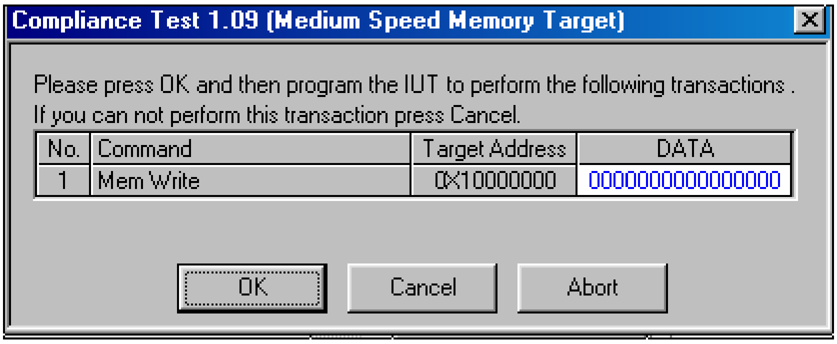
  In this test six transactions must be executed. The first is a memory read, the second is a memory write, the third is an I/O read, the fourth is an I/O write, the fifth is a configuration read and the last is a configuration write. All transactions have one data phase.



Compliance Test 1.09 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

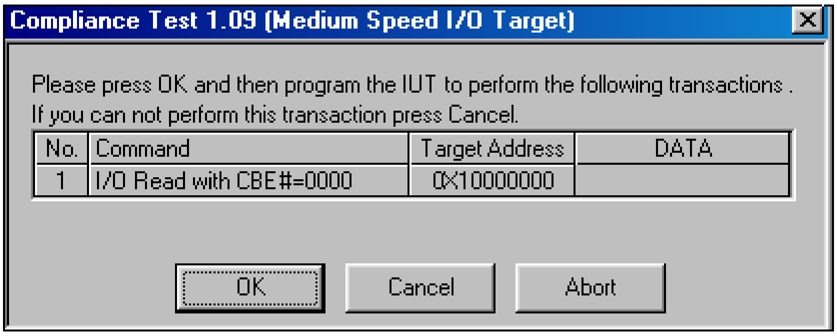
No.	Command	Target Address	DATA
1	Mem Read with CBE#=0000	0X10000000	



Compliance Test 1.09 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

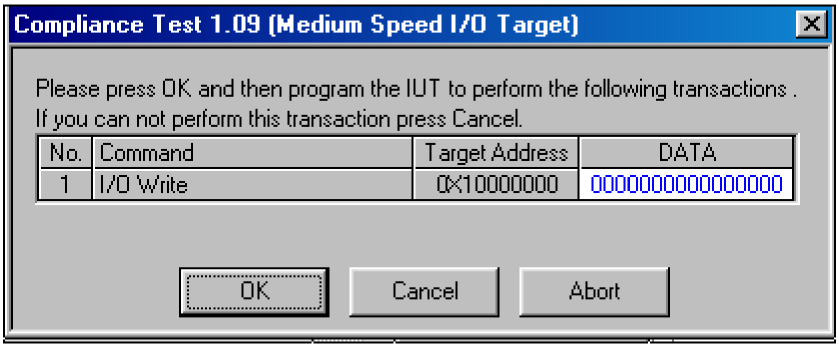
No.	Command	Target Address	DATA
1	Mem Write	0X10000000	0000000000000000



Compliance Test 1.09 (Medium Speed I/O Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

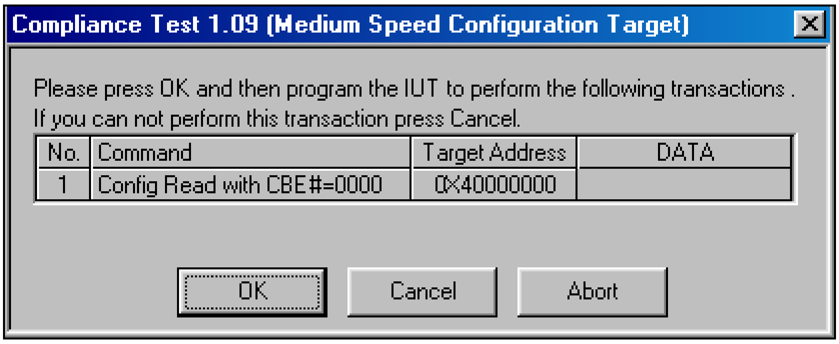
No.	Command	Target Address	DATA
1	I/O Read with CBE#=0000	0X10000000	



Compliance Test 1.09 (Medium Speed I/O Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

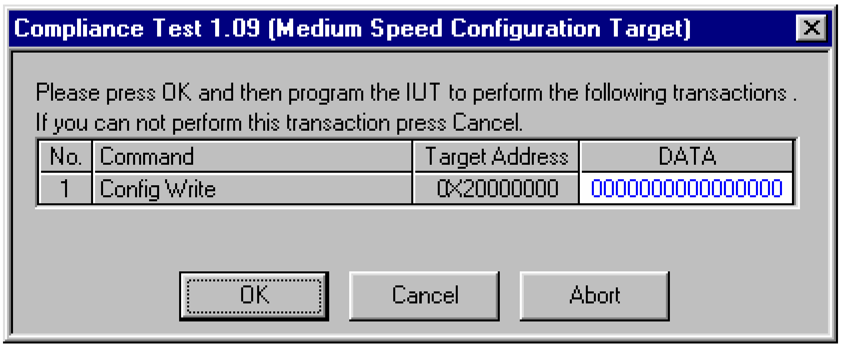
No.	Command	Target Address	DATA
1	I/O Write	0X10000000	0000000000000000



Compliance Test 1.09 (Medium Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Config Read with CBE#=0000	0X40000000	



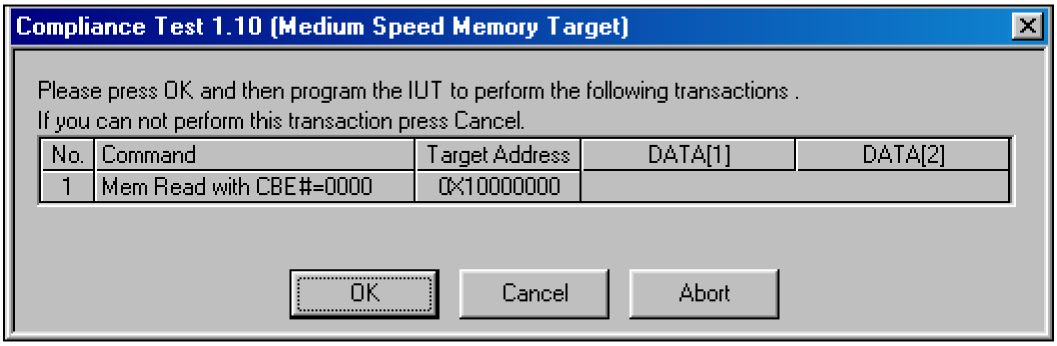
Compliance Test 1.09 (Medium Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA
1	Config Write	0X20000000	0000000000000000

- **1.10**
  PCI BUS DATA PARITY ERROR MULTI-DATA PHASE CYCLES

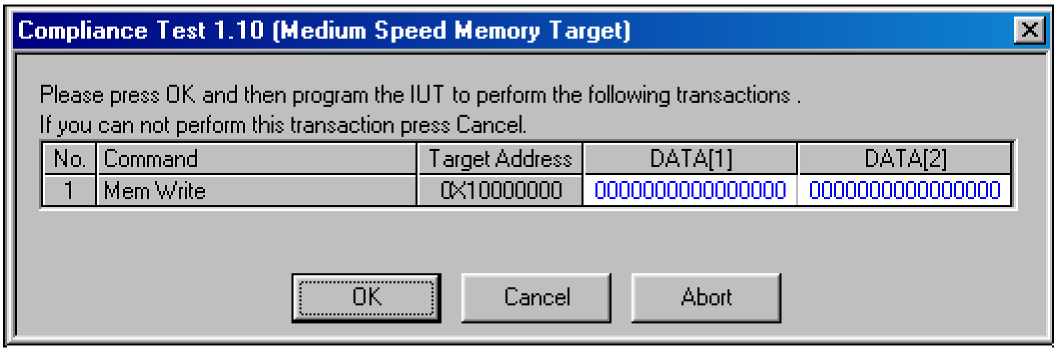
  In this test seven transactions must be executed. The first is a memory read, the second is a memory write, the third is a configuration read, the fourth is a configuration write, the fifth is a memory read multiple, the sixth is a memory read line and the last is a memory write & invalidate. All transactions have two data phases.



Compliance Test 1.10 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

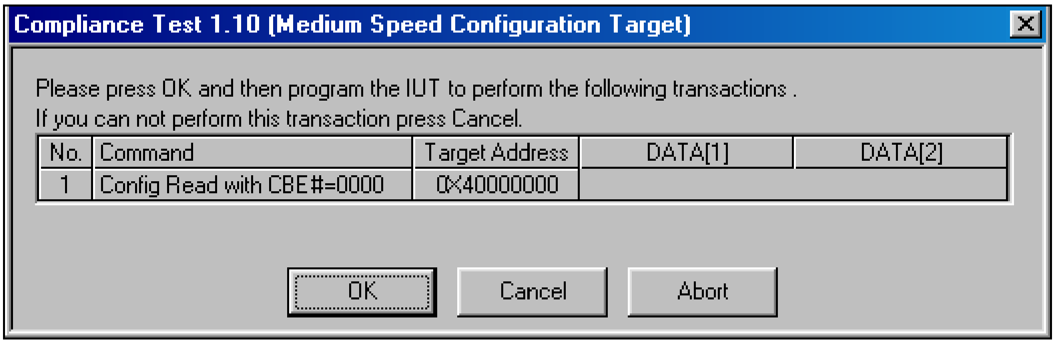
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read with CBE#=0000	0X10000000		



Compliance Test 1.10 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

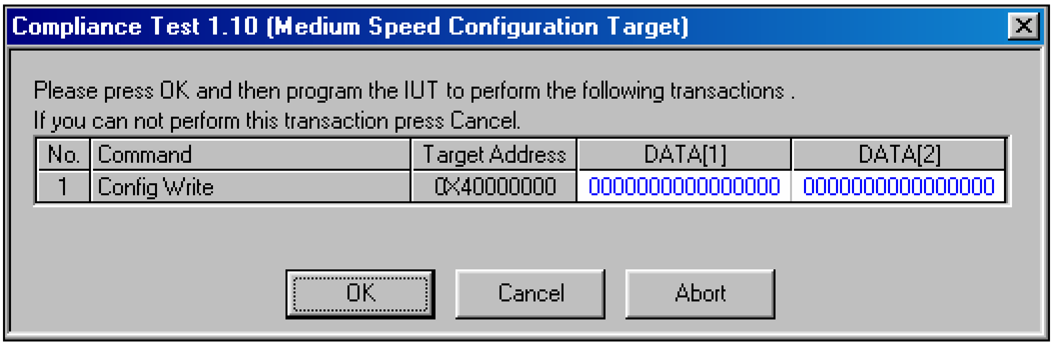
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write	0X10000000	0000000000000000	0000000000000000



Compliance Test 1.10 (Medium Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

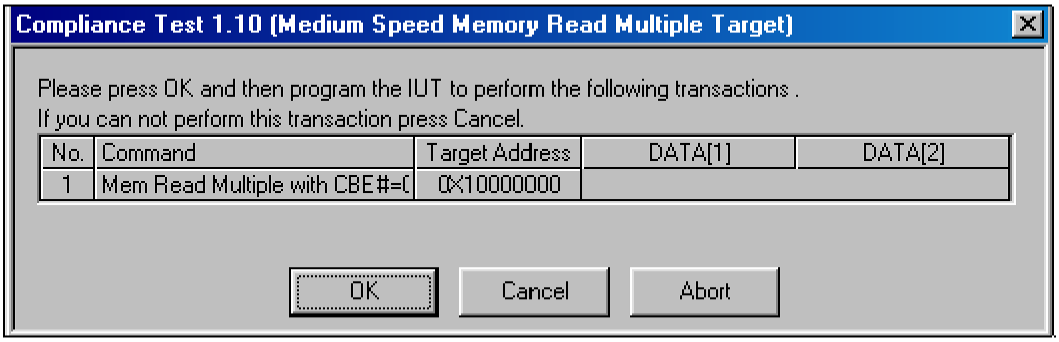
No.	Command	Target Address	DATA[1]	DATA[2]
1	Config Read with CBE#=0000	0X40000000		



Compliance Test 1.10 (Medium Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

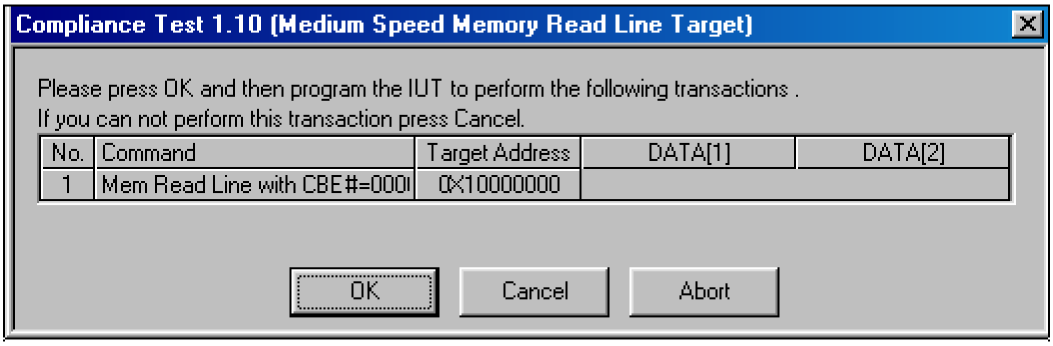
No.	Command	Target Address	DATA[1]	DATA[2]
1	Config Write	0X40000000	0000000000000000	0000000000000000



Compliance Test 1.10 (Medium Speed Memory Read Multiple Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

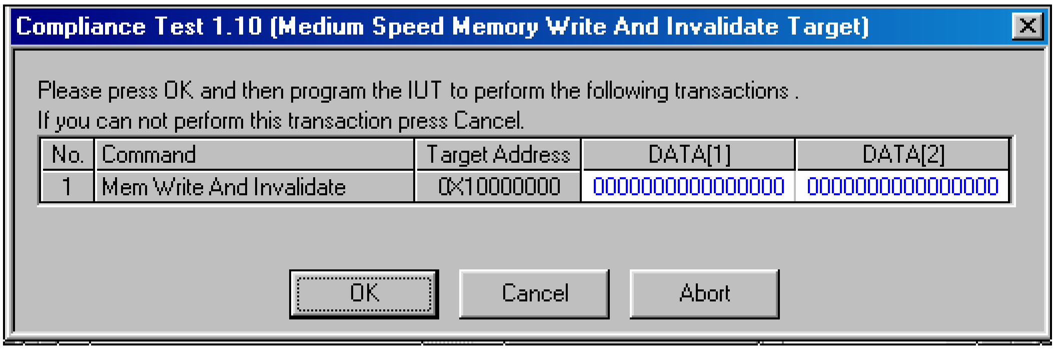
No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Multiple with CBE#=(	0X10000000		



Compliance Test 1.10 (Medium Speed Memory Read Line Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Read Line with CBE#=000	0X10000000		



Compliance Test 1.10 (Medium Speed Memory Write And Invalidate Target)

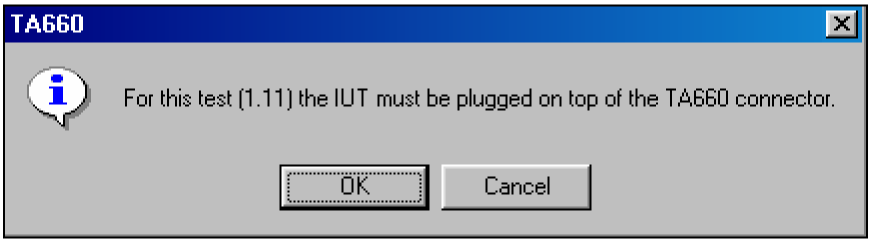
Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]
1	Mem Write And Invalidate	0X10000000	0000000000000000	0000000000000000

1.11
PCI BUS MASTER TIMEOUT

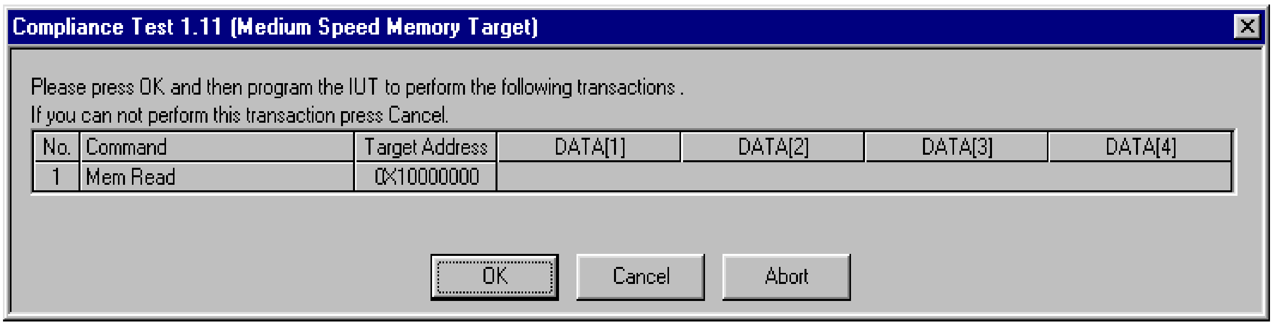
This test requires the IUT to be plugged on top of TA660. Therefore this test can only be done with PCI analyzers and not CPCI. The 1.11 test will not be executed by the software when user is using TA600C.

In this test the IUT must be plugged on the top connector of TA660. The requested transactions are similar to the test 1.10 with the exception that each transaction has four data phases.



TA660

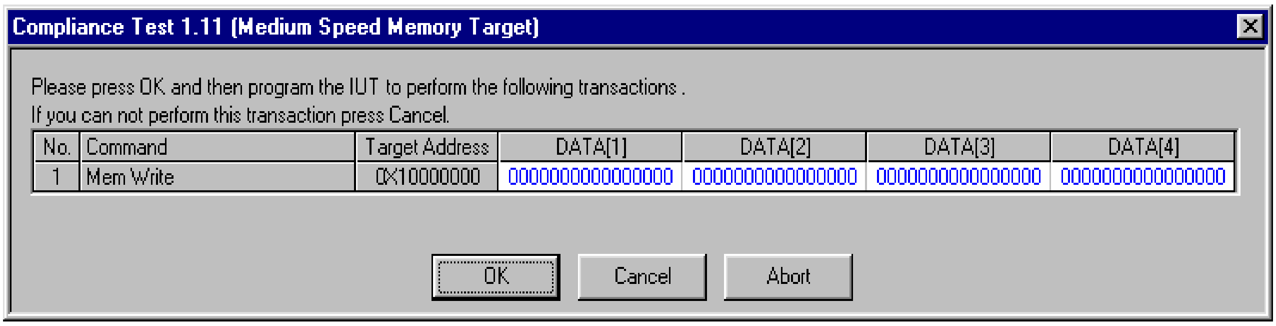
For this test (1.11) the IUT must be plugged on top of the TA660 connector.



Compliance Test 1.11 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

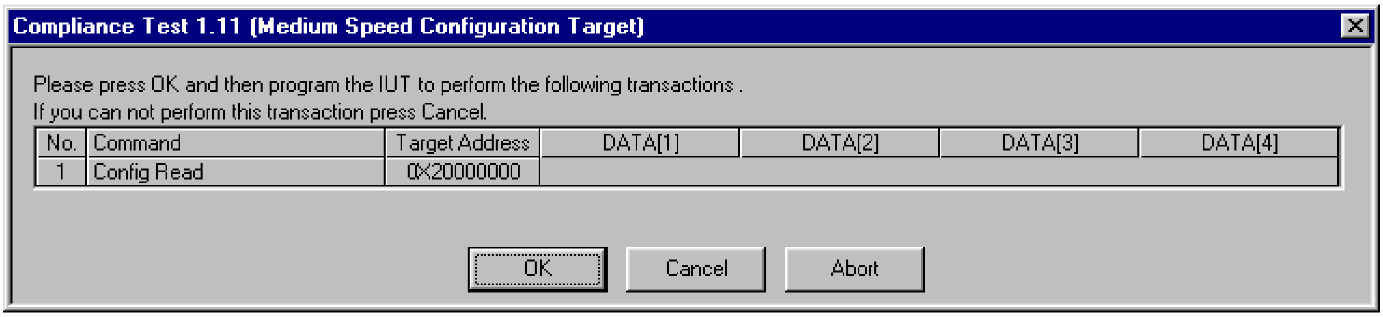
No.	Command	Target Address	DATA[1]	DATA[2]	DATA[3]	DATA[4]
1	Mem Read	0X10000000				



Compliance Test 1.11 (Medium Speed Memory Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

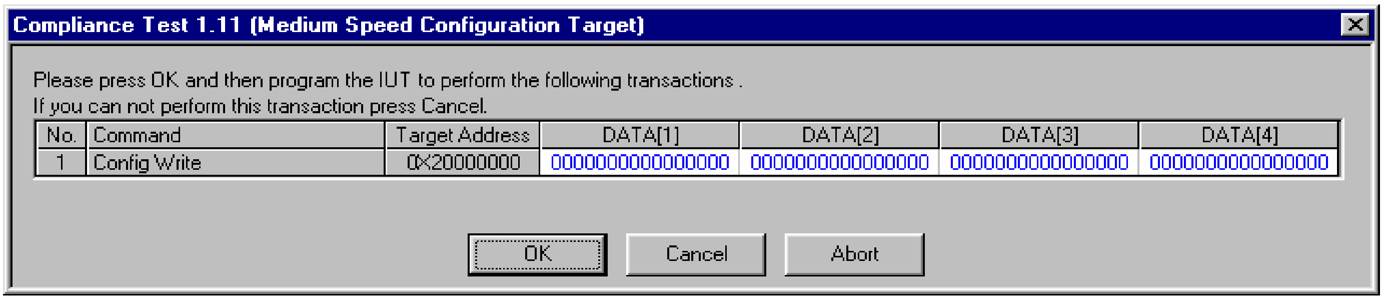
No.	Command	Target Address	DATA[1]	DATA[2]	DATA[3]	DATA[4]
1	Mem Write	0X10000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000



Compliance Test 1.11 (Medium Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

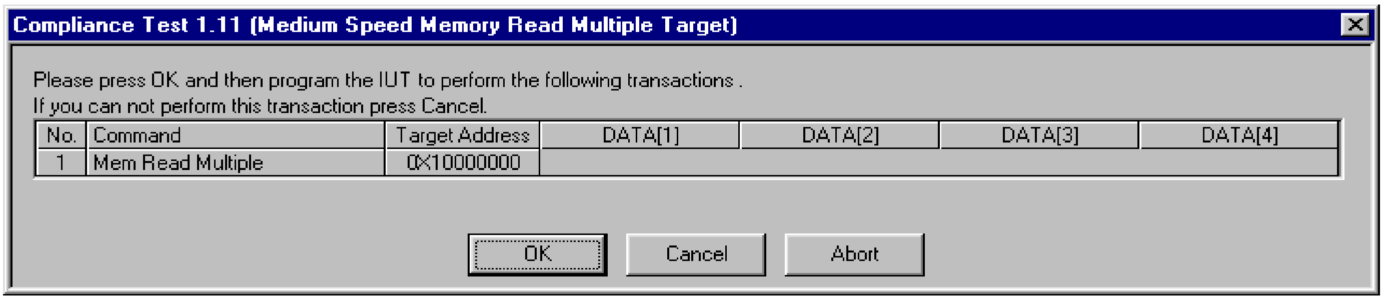
No.	Command	Target Address	DATA[1]	DATA[2]	DATA[3]	DATA[4]
1	Config Read	0X20000000				



Compliance Test 1.11 (Medium Speed Configuration Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

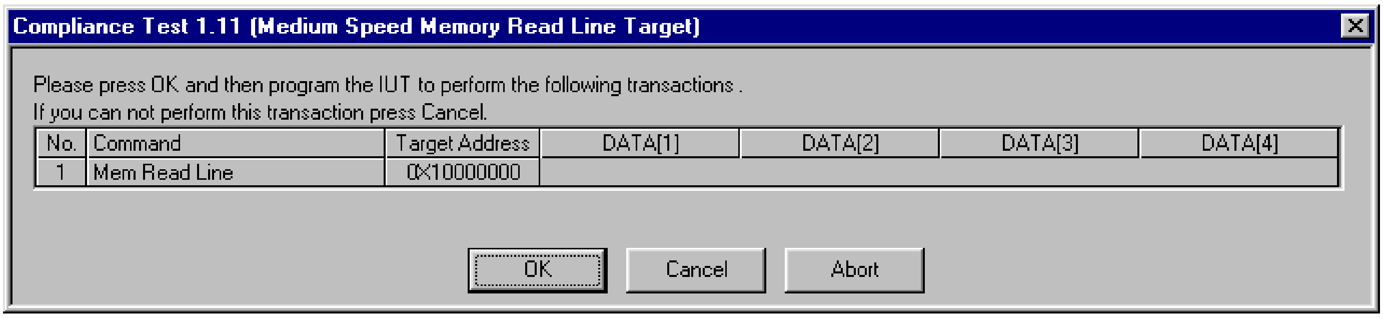
No.	Command	Target Address	DATA[1]	DATA[2]	DATA[3]	DATA[4]
1	Config Write	0X20000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000



Compliance Test 1.11 (Medium Speed Memory Read Multiple Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

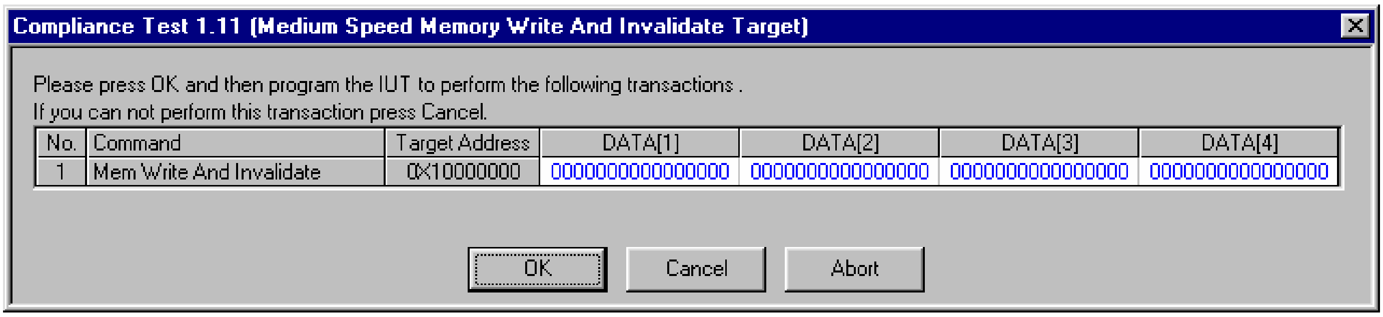
No.	Command	Target Address	DATA[1]	DATA[2]	DATA[3]	DATA[4]
1	Mem Read Multiple	0X10000000				



Compliance Test 1.11 (Medium Speed Memory Read Line Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]	DATA[3]	DATA[4]
1	Mem Read Line	0X10000000				



Compliance Test 1.11 (Medium Speed Memory Write And Invalidate Target)

Please press OK and then program the IUT to perform the following transactions .
If you can not perform this transaction press Cancel.

No.	Command	Target Address	DATA[1]	DATA[2]	DATA[3]	DATA[4]
1	Mem Write And Invalidate	0X10000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000

Below is a summary table of the MP_XX transactions:

Test	Command	Burst size	Data(s)	CBE#(s)
MP_02	Mem Write & Inv.	2	00000000-00000000	0000-0000
MP_03	Mem Write & Inv.	2	00000000-00000000	0000-0000
MP_04	Mem Write	1	00000000	0000
MP_05	Mem Read	1	00000000	0000
MP_06	Mem Read	3	00000000-00000000 00000000	0000-0000 0000
MP_07	Mem Read	3	00000000-00000000 00000000	0000-0000 0000
MP_08	Mem Read	2	00000000-00000000	0000-0000
MP_09	Mem Read	2	00000000-00000000	0000-0000
MP_11	Mem Write	2	00000000-00000000	1100-1100
MP_13	Mem Read	2	00000000-00000000	0000-0001
MP_14	Mem Read	3	00000000-00000000 00000000	0000-0000 0000
MP_15	Mem Read	3	00000000-00000000 00000000	0000-0000 0000
MP_16	Mem Read	3	00000000-00000000 00000000	0000-0000 0000
MP_17	Mem Read	1	00000000	0000
MP_18	Mem Read	1	00000000	0000
MP_19	Mem Read	1	00000000	0000
MP_20	Mem Read (1)	1	00000000	0000
	Mem Read (2)	1	00000000	0000
	Mem Read (3)	1	00000000	0000
MP_23	Mem Write	4	00000000-00000000 00000000-00000000	0000-0000 0000-0000
MP_24	Mem Write	1	00000000	0000
MP_25	Mem Write	1	00000000	0000
MP_28	Mem Read (1)	1	00000000	0000
	Mem Write (2)	1	98765431	0000
	Mem Write (3)	1	98765430	0000
	Mem Read (1)	1	00000000	0000

MP_29	Mem Write (2)	1	98765431	0000
	Mem Write (3)	1	98765430	0000
MP_30	Mem Read	1	00000000	0000
MP_31	Mem Read	3	00000000-00000000 00000000	0000-0000 0000
MP_32	Dual Address	1	00000000	0000

Below is a summary table of the 1.XX transactions.

The transactions with red color must be executed only when the test environment is a passive motherboard:

Test	Command	Burst size	Data(s)	CBE#(s)
1.01	Mem Read (1)	1	00000000	0000
	Mem Write (2)	1	00000000	0000
	Mem Read (3)	1	00000000	0000
	Mem Write (4)	1	00000000	0000
	Mem Read (5)	1	00000000	0000
	Mem Write (6)	1	00000000	0000
	Mem Read (7)	1	00000000	0000
	Mem Write (8)	1	00000000	0000
	I/O Read (9)	1	00000000	0000
	I/O Write (10)	1	00000000	0000
	I/O Read (11)	1	00000000	0000
	I/O Write (12)	1	00000000	0000
	I/O Read (12.1)	1	00000000	0000
	I/O Write (12.2)	1	00000000	0000
	I/O Read (12.3)	1	00000000	0000
	I/O Write (12.4)	1	00000000	0000
	Config Read (13)	1	00000000	0000
	Config Write (14)	1	00000000	0000
	Config Read (15)	1	00000000	0000
	Config Write (16)	1	00000000	0000
	Config Read (17)	1	00000000	0000
	Config Write (18)	1	00000000	0000
	Config Read (19)	1	00000000	0000
	Config Write (20)	1	00000000	0000
	Special Cycle	1	FFFFFFFF	0000

Test	Command	Burst size	Data(s)	CBE#(s)
1.02	Mem Read (1)	1	00000000	0000
	Mem Write (2)	1	00000000	0000
	Mem Read (3)	1	00000000	0000
	Mem Write (4)	1	00000000	0000
	Mem Read (5)	1	00000000	0000
	Mem Write (6)	1	00000000	0000
	I/O Read (7)	1	00000000	0000
	I/O Write (8)	1	00000000	0000
	I/O Read (9)	1	00000000	0000
	I/O Write (10)	1	00000000	0000
	I/O Read (10.1)	1	00000000	0000
	I/O Write (10.2)	1	00000000	0000
	Config Read (11)	1	00000000	0000
	Config Write (12)	1	00000000	0000
	Config Read (13)	1	00000000	0000
	Config Write (14)	1	00000000	0000
	Config Read (15)	1	00000000	0000
	Config Write (16)	1	00000000	0000

Test	Command	Burst size	Data(s)	CBE#(s)
1.03	Mem Read (1)	1	00000000	0000
	Mem Write (2)	1	00000000	0000
	Mem Read (3)	1	00000000	0000
	Mem Write (4)	1	00000000	0000
	Mem Read (5)	1	00000000	0000
	Mem Write (6)	1	00000000	0000
	I/O Read (7)	1	00000000	0000
	I/O Write (8)	1	00000000	0000
	I/O Read (9)	1	00000000	0000
	I/O Write (10)	1	00000000	0000
	I/O Read (10.1)	1	00000000	0000
	I/O Write (10.2)	1	00000000	0000
	Config Read (11)	1	00000000	0000
	Config Write (12)	1	00000000	0000
	Config Read (13)	1	00000000	0000
	Config Write (14)	1	00000000	0000
	Config Read (15)	1	00000000	0000
	Config Write (16)	1	00000000	0000
1.04	Mem Read (1)	1	00000000	0000
	Mem Write (2)	1	00000000	0000
	Mem Read (3)	1	00000000	0000
	Mem Write (4)	1	00000000	0000
	Mem Read (5)	1	00000000	0000
	Mem Write (6)	1	00000000	0000
	I/O Read (7)	1	00000000	0000
	I/O Write (8)	1	00000000	0000
	I/O Read (9)	1	00000000	0000
	I/O Write (10)	1	00000000	0000
	I/O Read (10.1)	1	00000000	0000
	I/O Write (10.2)	1	00000000	0000
	Config Read (11)	1	00000000	0000
	Config Write (12)	1	00000000	0000
	Config Read (13)	1	00000000	0000
	Config Write (14)	1	00000000	0000
	Config Read (15)	1	00000000	0000
	Config Write (16)	1	00000000	0000

Test	Command	Burst size	Data(s)	CBE#(s)
1.05	Mem Read (1)	2	00000000-00000000	0000-0000
	Mem Write (2)	2	00000000-00000000	0000-0000
	Mem Read (3)	2	00000000-00000000	0000-0000
	Mem Write (4)	2	00000000-00000000	0000-0000
	Mem Read (5)	2	00000000-00000000	0000-0000
	Mem Write (6)	2	00000000-00000000	0000-0000
	Config Read (7)	2	00000000-00000000	0000-0000
	Config Write (8)	2	00000000-00000000	0000-0000
	Config Read (9)	2	00000000-00000000	0000-0000
	Config Write (10)	2	00000000-00000000	0000-0000
	Config Read (11)	2	00000000-00000000	0000-0000
	Config Write (12)	2	00000000-00000000	0000-0000
	Mem Read Mul.(13)	2	00000000-00000000	0000-0000
	Mem Read Mul.(14)	2	00000000-00000000	0000-0000
	Mem Read Mul.(15)	2	00000000-00000000	0000-0000
	Mem Read Line.(16)	2	00000000-00000000	0000-0000
	Mem Read Line.(17)	2	00000000-00000000	0000-0000
	Mem Read Line.(18)	2	00000000-00000000	0000-0000
	Mem Write&Inv.(19)	2	00000000-00000000	0000-0000
	Mem Write&Inv.(20)	2	00000000-00000000	0000-0000
	Mem Write&Inv.(21)	2	00000000-00000000	0000-0000
1.06	Mem Read (1)	2	00000000-00000000	0000-0000
	Mem Write (2)	2	00000000-00000000	0000-0000
	Mem Read (3)	2	00000000-00000000	0000-0000
	Mem Write (4)	2	00000000-00000000	0000-0000
	Mem Read (5)	2	00000000-00000000	0000-0000
	Mem Write (6)	2	00000000-00000000	0000-0000
	Config Read (7)	2	00000000-00000000	0000-0000
	Config Write (8)	2	00000000-00000000	0000-0000
	Config Read (9)	2	00000000-00000000	0000-0000
	Config Write (10)	2	00000000-00000000	0000-0000
	Config Read (11)	2	00000000-00000000	0000-0000
	Config Write (12)	2	00000000-00000000	0000-0000
	Mem Read Mul.(13)	2	00000000-00000000	0000-0000
	Mem Read Mul.(14)	2	00000000-00000000	0000-0000
	Mem Read Mul.(15)	2	00000000-00000000	0000-0000
	Mem Read Line.(16)	2	00000000-00000000	0000-0000
	Mem Read Line.(17)	2	00000000-00000000	0000-0000
	Mem Read Line.(18)	2	00000000-00000000	0000-0000
	Mem Write&Inv.(19)	2	00000000-00000000	0000-0000
	Mem Write&Inv.(20)	2	00000000-00000000	0000-0000
	Mem Write&Inv.(21)	2	00000000-00000000	0000-0000

Test	Command	Burst size	Data(s)	CBE#(s)
1.07	Mem Read (1)	2	00000000-00000000	0000-0000
	Mem Write (2)	2	00000000-00000000	0000-0000
	Mem Read (3)	2	00000000-00000000	0000-0000
	Mem Write (4)	2	00000000-00000000	0000-0000
	Mem Read (5)	2	00000000-00000000	0000-0000
	Mem Write (6)	2	00000000-00000000	0000-0000
	Config Read (7)	2	00000000-00000000	0000-0000
	Config Write (8)	2	00000000-00000000	0000-0000
	Config Read (9)	2	00000000-00000000	0000-0000
	Config Write (10)	2	00000000-00000000	0000-0000
	Config Read (11)	2	00000000-00000000	0000-0000
	Config Write (12)	2	00000000-00000000	0000-0000
	Mem Read Mul.(13)	2	00000000-00000000	0000-0000
	Mem Read Mul.(14)	2	00000000-00000000	0000-0000
	Mem Read Mul.(15)	2	00000000-00000000	0000-0000
	Mem Read Line.(16)	2	00000000-00000000	0000-0000
	Mem Read Line.(17)	2	00000000-00000000	0000-0000
	Mem Read Line.(18)	2	00000000-00000000	0000-0000
	Mem Write&Inv.(19)	2	00000000-00000000	0000-0000
	Mem Write&Inv.(20)	2	00000000-00000000	0000-0000
	Mem Write&Inv.(21)	2	00000000-00000000	0000-0000
1.08	Mem Read (1)	3	00000000-00000000 00000000	0000-0000 0000
	Mem Write (2)	3	00000000-00000000 00000000	0000-0000 0000
	Mem Read Mul.(3)	3	00000000-00000000 00000000	0000-0000 0000
	Mem Read Line.(4)	3	00000000-00000000 00000000	0000-0000 0000
	Mem Write&Inv.(5)	3	00000000-00000000 00000000	0000-0000 0000
1.09	Mem Read (1)	1	00000000	0000
	Mem Write (2)	1	00000000	0000
	I/O Read (3)	1	00000000	0000
	I/O Write (4)	1	00000000	0000
	Config Read (5)	1	00000000	0000
	Config Write (6)	1	00000000	0000

Test	Command	Burst size	Data(s)	CBE#(s)
1.10	Mem Read (1)	2	00000000-00000000	0000-0000
	Mem Write (2)	2	00000000-00000000	0000-0000
	Config Read (3)	2	00000000-00000000	0000-0000
	Config Write (4)	2	00000000-00000000	0000-0000
	Mem Read Mul.(5)	2	00000000-00000000	0000-0000
	Mem Read Line.(6)	2	00000000-00000000	0000-0000
	Mem Write&Inv.(7)	2	00000000-00000000	0000-0000
1.11	Mem Read (1)	4	00000000-00000000 00000000-00000000	0000-0000 0000-0000
	Mem Write (2)	4	00000000-00000000 00000000-00000000	0000-0000 0000-0000
	Config Read (3)	4	00000000-00000000 00000000-00000000	0000-0000 0000-0000
	Config Write (4)	4	00000000-00000000 00000000-00000000	0000-0000 0000-0000
	Mem Read Mul.(5)	4	00000000-00000000 00000000-00000000	0000-0000 0000-0000
	Mem Read Line.(6)	4	00000000-00000000 00000000-00000000	0000-0000 0000-0000
	Mem Write&Inv.(7)	4	00000000-00000000 00000000-00000000	0000-0000 0000-0000